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Hot Electron Induced Punchthrough in Submicron PMOSFETs

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Hot carrier reliability in submicron PMOSFETs has been investigated. It has been found that in submicron p-channel transistors the punchthrough voltage is seriously reduced due to Hot Electron Induced Punchthrough (HEIP). HEIP effect results from the effective channel length reduction due to hot electron injection into the gate oxide near the drain. Such hot electron injection is most significant at a low stress gate voltage, since hot electrons generated by impact ionization are then easily emitted into the gate oxide. Worst case analysis of the experimental data shows short device lifetime (< 1 day) for 0.8 μm gate length PMOSFETs due to the HEIP effect.

1. Introduction

It is well known that hot carrier induced device degradation is a serious problem in fabricating reliable short n-channel MOSFETs, and many studies of this phenomenon have been reported [1]-[3]. However, hot carrier induced problems in short channel PMOSFETs have not been investigated in detail and have not so far been viewed as very important in device reliability. This is however not valid particularly for submicron PMOSFETs needed for future CMOS VLSI operating at 5 volt supply. The work described here shows that punchthrough voltages are significantly reduced by hot electron injection into the gate oxide for submicron p-channel MOSFETs. This problem is serious because high punchthrough voltages are hard to obtain for p-channel MOSFETs in CMOS integrated circuits due to the buried channel nature of the FETs when n+ polysilicon gates are used. Punchthrough voltage reduction due to hot carrier injection further aggravates the problem. The new phenomenon described here, Hot Electron Induced Punchthrough (HEIP), represents the most severe degradation mechanism limiting device lifetime, and may place a fundamental limitation on submicron PMOSFET long-term reliability.

2. Experiments

The measured p-channel devices were fabricated using a typical polysilicon gate n-well CMOS process. The n-well depth was ~1.5 μm and the n-well surface concentration (phosphorus) was $4x10^{16}$ cm^{-3}. Effective channel lengths ranged from 0.4 μm to 1.6 μm. The gate oxide thickness was 21 nm and the source/drain junction depth was 0.35 μm. The devices were stressed with drain voltage varying from -6 V to -10 V. The gate voltage during stressing was set to a low value (-1.25V) since this gives both a maximum gate current and a maximum stress-induced threshold voltage shift, although the substrate current at this bias is not maximum. This contrasts with the results reported for NMOSFETs, in which device degradation is worst at the gate voltage corresponding to the largest substrate current. The maximum substrate current measured from the PMOSFETs was at the gate voltage near -3 V, the same magnitude as for NMOSFETs. The present measurements also include interchanging source and drain terminals after stressing. This is a sensitive method for reflecting characteristic changes due to hot carrier injection [4]. It also simulates real operating condition when the device is used as a pass transistor.

3. Results and Discussion

The effect of hot carrier injection on p-channel device characteristics differs considerably from the hot carrier effects observed in n-channel devices. In particular, the transconductance, g_m, of a p-channel device increases as a result of stress, while the magnitude of the threshold voltage decreases. This contrasts with the decrease in transconductance and increase in threshold voltage widely reported for n-channel devices. These differences may be explained as follows. In n-channel transistors, both channel hot electrons and hot holes and electrons generated by impact ionization play an important role in hot carrier induced device reliability [2]-[3]. However, in a p-channel device, it is probable that only hot electrons generated by impact ionization have a significant role. Electrons are more easily injected into the gate oxide than holes due to the lower barrier height, and at low gate voltages the gate to channel field near the drain aids this injection. Thus, the gate current measured in PMOS devices reaches a peak at low gate bias. The high oxide barrier height for holes stops significant injection of either channel hot holes or hot holes generated by secondary impact ionization, and these carriers are simple collected by the drain.

Figure 1 illustrates the increase in transconductance of a p-channel transistor with an effective channel length, L_{eff}, of 0.6 μm due to stressing at V_D = -8V and V_G = -1.25V for 100 minutes. The characteristics of an unstressed

device with L_{eff} = 0.4 μm are also shown for comparison. These results can be explained by hot electron injection near the drain junction according to the mechanism described above. Hot electrons generated by impact ionization are accelerated towards the gate dielectric by the gate field and become trapped in the gate oxide near the drain. These trapped electrons reduce the channel electric field and cause the substrate current to decrease, as shown in Fig.2. However, this is not the limiting effect determining PMOSFET reliability. What is really important is that the trapped electrons invert the silicon surface near the drain resulting in an effective extension of the p+ drain region. Consequently, the effective channel length, L_{eff}, decreases in the low gate voltage region. Thus, a stressed p-channel device may be modelled as two transistors with different thresholds in series. Depending on the amount of electrons trapped, the threshold voltage of the second transistor can become depletion mode. The g_m vs gate voltage relation, calculated using such a model, is also shown in Fig.1. Excellent agreement between the experimental curve and the calculated one has been observed. L_{eff} reduction at low gate voltage is undesirable for short-channel PMOS devices since it gives rise to a poor subthreshold characteristic and consequently a reduction in the source-drain punchthrough voltage. Subthreshold characteristics before and after stressing are shown in Fig.3. The initial characteristic before stressing is good, but after stressing there is a drastic degradation due to channel shortening and HEIP, particularly when source and drain are reversed. Degradation of subthreshold voltage swing, S, with stressing time is shown in Fig.4. Initial L_{eff} and S values of this device are 0.6 μm and 105 mV/dec, respectively. It is clear from the figure that the degradation of sub-threshold slope after stressing is very large.

Degradation of punchthrough voltage, V_{PT}, with stressing time is shown in Fig.5. Punchthrough voltage was defined as a drain voltage which gives rise to a drain current of 1 μA (I_{PT} = 1 μA) at zero gate voltage. For devices with L_{eff} = 0.6 μm, punchthrough voltage rapidly decreases to less than the supply voltage, 5 V. Such punchthrough voltage reduction is due to the reduction of effective channel length caused by hot electron injection. Punchthrough voltages vs. effective channel length before and after stressing are shown in Fig.6. It is clear that punchthrough voltage is strongly reduced in short channel FETs due to the HEIP effect after stressing. The HEIP-induced L_{eff} reduction is ~0.15 μm, which is consistent with the value obtained from the transconductance increase using the two transistor model.

Threshold voltage defined by a current which lies in the subthreshold region is more sensitive to characteristic changes caused by hot electron injection. In this work, the threshold voltage is defined as the gate voltage which gives rise to a drain current of 10 nA at a drain voltage of -5 V. This measurement is sensitive to changes in punchthrough as well as the more conventional extrapolated threshold, and so is appropriate for evaluating HEIP. The threshold voltage shift ΔV_{th} with stressing time is shown in Fig.7. The initial threshold voltage before stressing was -0.55 V. As shown in Fig.7, the threshold voltage shifts significantly towards positive values after stressing. The stress time which corresponds to a 100 mV threshold voltage shift is defined as the device lifetime. Such lifetimes for devices with L_{eff} = 0.6 μm and 0.8 μm are plotted versus the reciprocal stressing drain voltage in Fig.8. Lifetimes defined by 10% g_m increase are also plotted on the figure. Device lifetime is about one year for a PMOSFET with L_{eff} = 0.8 μm at the worst supply voltage (5V + 10% variation). It is less than 10 days for a PMOSFET with L_{eff} = 0.6 μm! Implanting phosphorus into the substrate under the channel as a punchthrough stopper improves the device lifetime as shown in Fig.9. However, it is still less than 100 days for a PMOSFET with L_{eff} = 0.6 μm. The device with L_{eff} = 0.4 μm, shows an extremely short lifetime (< 1 day). These results suggest that conventional p-channel MOSFETs may not be appropriate for 0.8 μm technology operating at 5 volt. LDD (Lightly Doped Drain) structures may be necessary for p-channel devices as well as for n-channel devices in a 0.8 μm CMOS technology. While LDD structures are effective in reducing impact ionization for n-channel devices, they alleviate HEIP for p-channel devices by reducing hot electron injection.

4. Summary

Degradation of device characteristics by hot carrier injection in submicron PMOSFET has been investigated. We found that punchthrough voltage is seriously reduced as a result of channel shortening by hot electron injection. This hot electron induced punchthrough (HEIP) in submicron p-channel transistors can place a fundamental limit on reliability of scaled devices. Experiments show short lifetime (< 10 days) for 0.6 μm p-channel devices according to the worst case measurement criterion established based on the HEIP effect. Consequently, for submicron PMOSFET with 5V supply, improved drain structures such as LDD may be necessary for reliable CMOS VLSI circuits.

Acknowledgment

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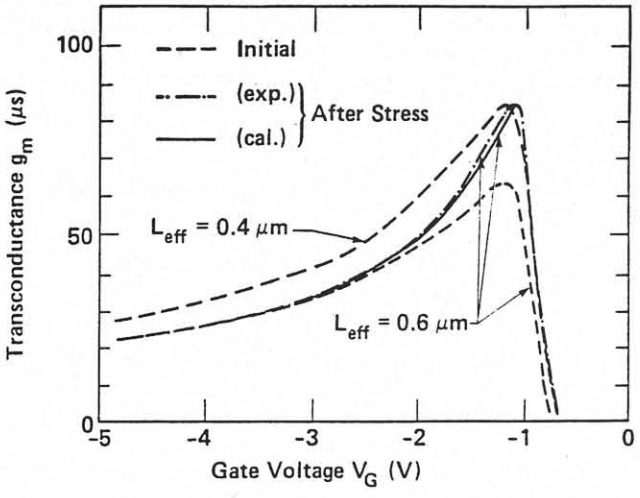

Fig. 1 Transconductance vs gate voltage relations before and after stressing for 100 minites. Stressing drain and gate voltages are -8 V and -1.25 V, respectively.

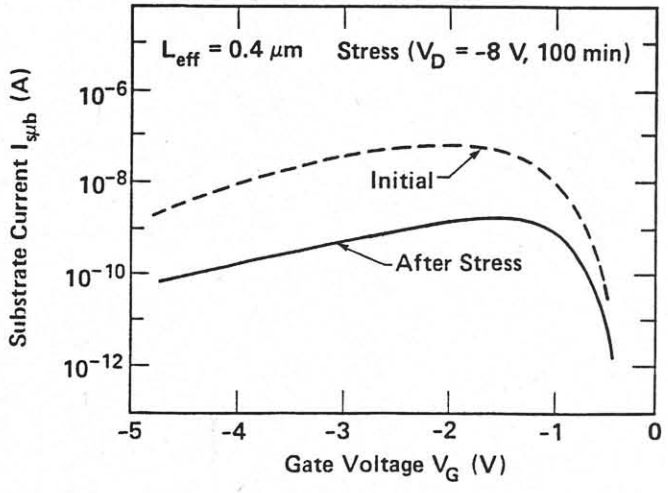

Fig. 2 Substrate current as a function of gate voltage before and after stressing.

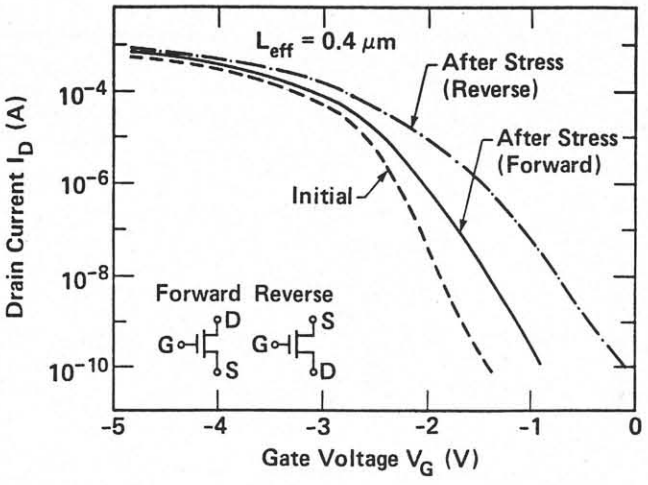

Fig. 3 Drain current as a function of gate voltage before and after stressing.

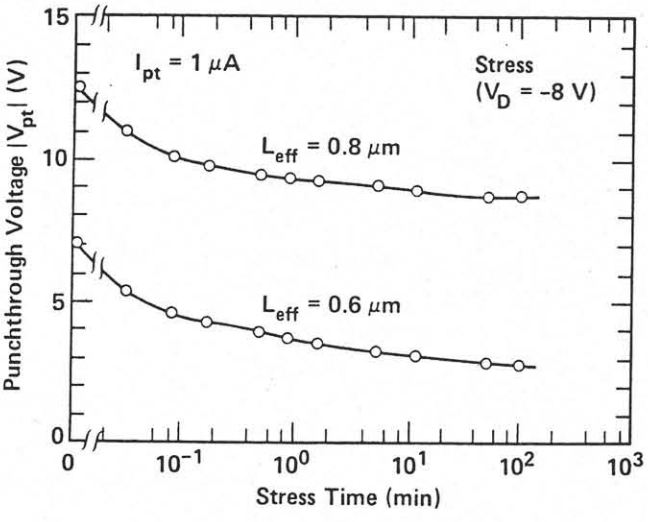

Fig. 4 Change of subthreshold voltage swing, S, with stressing time.

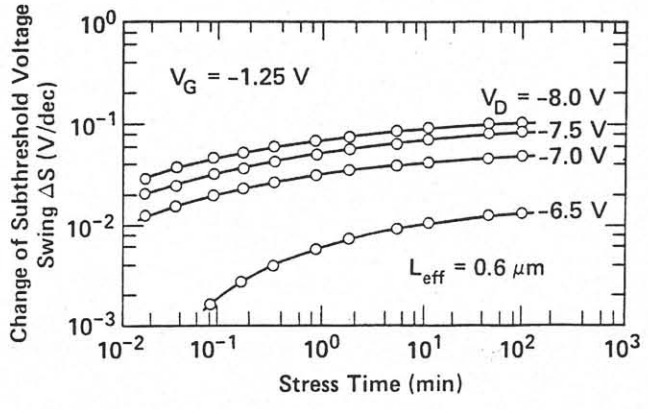

Fig. 5 Punchthrough voltage reduction with stressing time.

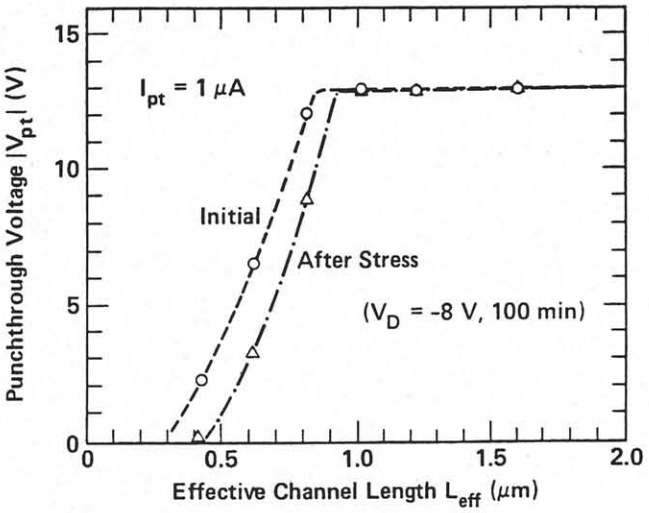

Fig. 6 Punchthrough voltage vs effective channel length relations before and after stressing.

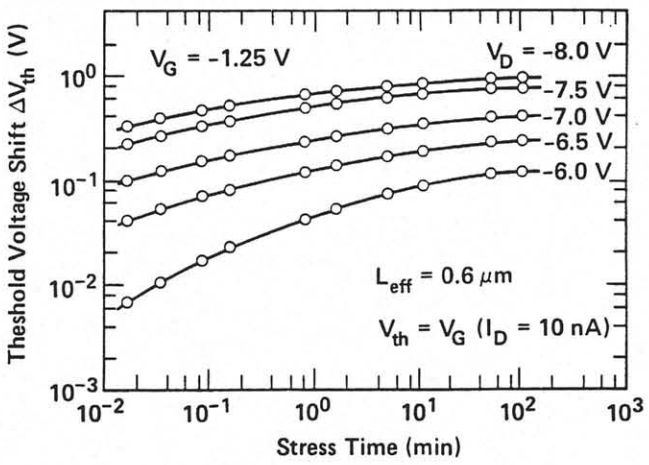

Fig. 7 Threshold voltage shift with stressing time.

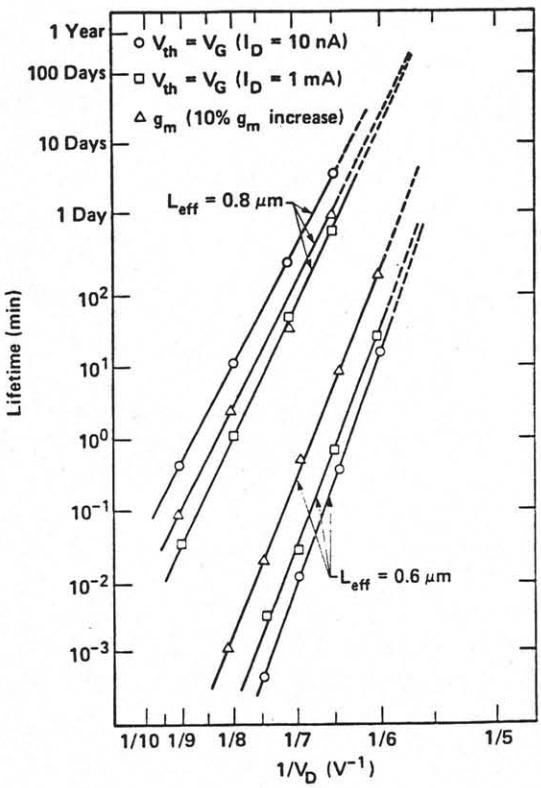

Fig.8 Device lifetime vs reciprocal stressing drain voltage for PMOSFET with no punchthrough stopper.

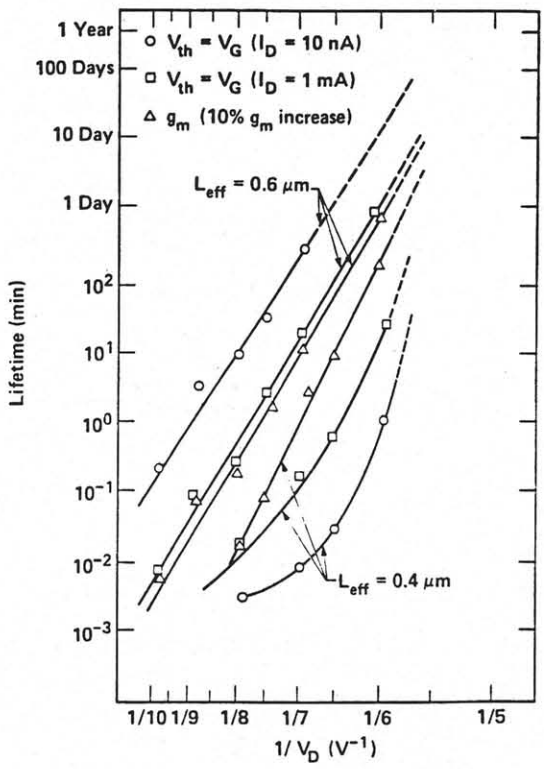

Fig.9 Device lifetime vs reciprocal stressing drain voltage for PMOSFET with punchthrough stopper.