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New Degradation Phenomena Induced by Ion- Implantation Channeling in Short Channel Transistors

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We studied the threshold voltage degradation in MOSFETs caused by the ion-channeling through the poly-silicon gate in the low acceleration source/drain ion-implantation process, and investigated the influence of the degradation phenomena on the VLSI circuit operation. It was clarified that the short channel transistor is much more sensitive to the ion channeling than the long channel transistor, which provides new problems of small size transistor design in VLSI circuits.

1. Introduction

The ion channeling through the poly-silicon gate in the self-aligned source/drain ion-implantation process causes the degradation of the device characteristics, such as flat band voltage and threshold voltage. Several analyses of the ion-implantation channeling have been reported as a function of acceleration voltage or stopping oxide thickness in high acceleration energy ion-implantation[1,2]. However, even in the much lower acceleration energy ion-implantation, we observed the threshold voltage, V_{th}, degradation in short channel MOSFETs. This phenomenon doesn't always occur in all the transistors, but only a few transistors degrade, unlike the case of high acceleration energy, where all transistors degrade. The probability of degraded transistors rapidly increases with decreasing the channel length. This degradation phenomenon becomes a difficult problem in device miniaturization. On the other hand, the Lightly Doped Drain (LDD) structure transistor is the most promising for device design to achieve reliable short channel transistors. If stopping layer, such as resist mask, is formed on the poly-silicon gate, the degradation is suppressed. However, in case of the LDD process [3], no resist mask can be used at the source/drain implantation process. The stopping oxide mask formed by the oxidation of the poly-silicon gate itself can be used, but can't control the gate length precisely. So the short channel transistor with the LDD structure is susceptible to ion-implantation channeling.

In this paper, we report the results of investigation on the degradation phenomena of short channel transistors induced by the ion-implantation channeling, and the influence of the phenomena on the VLSI circuit operation by the use of experiments and simulations.

2. Degradation phenomena of short channel MOSFETs

2.1 Experiments and results

A large number of n-channel transistors were fabricated by a conventional MOSFET process, where arsenic source/drain ion was implanted at a dose of 3×10^{15} cm^{-2} by 50 keV. Both the sample with thick stopping oxide (1200 Å) by oxidation of poly-silicon gate and the sample without the oxide on the poly-silicon gate, at source/drain ion implantation process, were prepared. Even in case of the sample without stopping oxide, arsenic ion concentration at the channel surface is estimated to be of much lower value than channel boron profile by LSS theory.[4] Figure 1 shows the threshold voltage, V_{th}, distribution among about 500 transistors in both cases of long channel (L=20μm) transistors and short channel (L=1.2μm) ones. For the long channel transistors, as shown in Fig.1-(a), there is no large difference between the sample with stopping oxide and the one

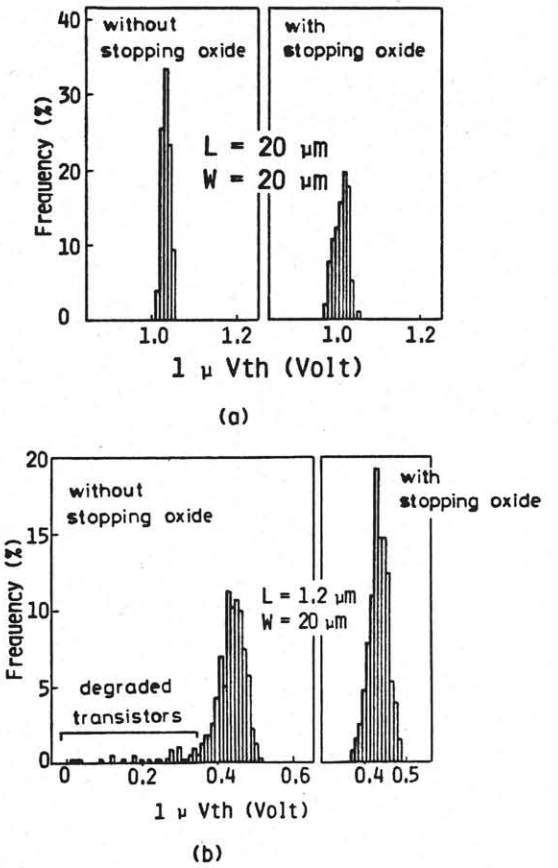

Fig.1 Threshold voltage, V_{th}, distribution: (a) long channel (L=20μm) MOSFETs, (b) short channel (L=1.2μm) MOSFETs. The left-hand figure is the case without stopping oxide and the right-hand one is that with stopping oxide.

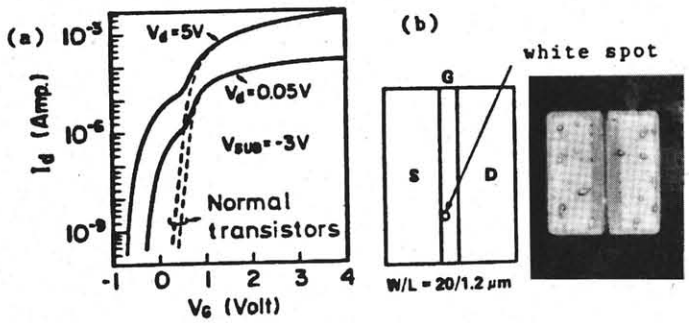

Fig.2 (a) Id-Vg characteristics of a degraded transistor, (b) Microphotograph of the surface, after stain etching, of the degraded transistor.

without the oxide. However, in case of short channel transistors as shown in Fig.1-(b), a few degraded transistors with notable decrease of V_{th} were observed in the samples without the stopping oxide. Figure 2-(a) shows the typical I_d-V_g characteristics of the degraded transistor. A large hump structure appears in the subthreshold characteristics. We removed the layer of oxide and poly-silicon on the degraded transistors by hydrofluoric acid, and etched the surface by stain etchant. The microphotograph of the surface is shown in Fig.2-(b). It is interesting to see that a small white spot is observed on the channel region in all the degraded transistors. This spot indicates the existence of diffusion spot of n-type impurity, whose concentration is more than 10^{17} cm^{-3}.[5]

2.2 Degradation mechanism

From the result in Fig.2 and the fact that the occurrence frequency of degraded transistors is in proportion to the channel width, it is possible to describe the degraded transistor by the parallel circuit, which consists of a normal transistor (Tr.1) with wide channel width and a degraded transistor (Tr.2) with narrow channel width of the white spot size, as shown in Fig.3. The Tr.2 has lower V_{th} than Tr.1, owing to the diffusion of n-type impurity. One may expect that the diffusion of n-type impurity is due to the following phenomena.

1) Anomalous diffusion of phosphorus in poly-silicon gate to the channel surface in subsequent thermal process.

2) Anomalous diffusion of implanted arsenic in poly-silicon gate to the channel surface in subsequent thermal process.

3) Ion channeling of implanted arsenic.

The first case is incorrect because of the fact that there is a large difference between the two cases in Fig.1-(b) regardless of the same phosphorus concentration and much the same thermal process flow. The second case is also wrong due to the following experimental results. First, arsenic ion was implanted on the poly-silicon, and the poly-silicon and gate oxide were removed completely. Then, MOSFET was fabricated on the same surface by a coventional process, where arsenic source/drain implanted ion was blocked using resist mask on the poly-silicon gate. However, degraded transistors appeared in the same

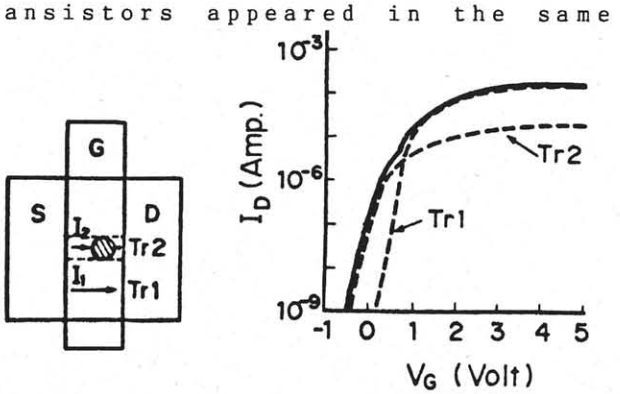

Fig.3 Model of degraded transistor: hatched circle shows the n-type diffusion spot.

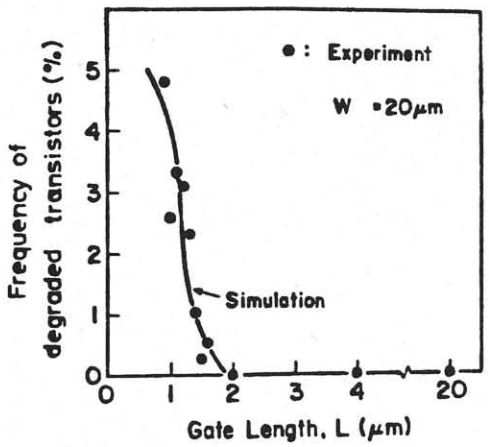

Fig.4 Occurrence frequency of degraded ($|(V_{th}$ shift)$|>0.1V$) transistors vs. poly-silicon gate length.

probability. So the second case is incorrect. Therefore, it is the most reasonable that the diffusion spot of n-type impurity in the channel is due to the ion-implantation channeling. Figure 4 shows the occurrence frequency of degraded transistors as a function of gate length. The solid line is simulated using the two-dimensional device simulator, MOS2C[6], and Transmission Electron Microscope (TEM) observation of the poly-silicon grain size. It is important to note that the occurrence frequency of degraded transistors increases rapidly with decrease of the gate length.

2.3 Channeling characteristics

Figure 5 represents the relation between the grain size of gate poly-silicon and the occurrence frequency of degraded transistors, where phosphorus source/drain ion was implanted at a dose of 1×10^{15} cm^{-2} by 40 keV. The grain size of the poly-silicon is distributed. The horizontal axis is the mean value measured by TEM observation. The ion channeling is suppressed by the use of the mean grain size smaller than 0.1 μm. Figure 6 shows the occurrence frequency of degraded transistors as a function of acceleration energy of ion-implantation. For the short channel (L=1.2μm), there is a large dependence of acceleration energy, while there is no dependence for the long channel (L=20μm) in the energy region lower than 80 keV. If the thick stopping oxide on the gate is formed by the oxidation of the poly-silicon gate, the ion channeling is suppressed. However, this method is unsuitable for submicron transistors because of the poor controlability of the gate length.

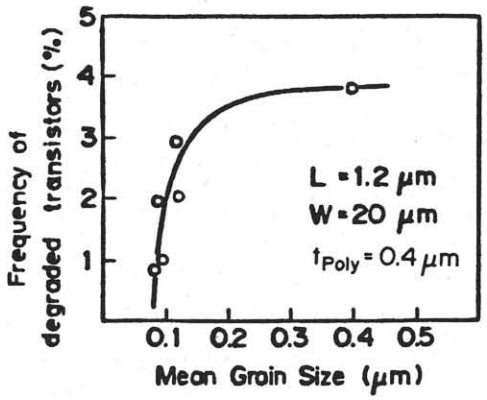

Fig.5 Frequency of degraded ($|(V_{th}$ shift)$|>0.1V$) transistors vs. mean grain size of poly-silicon gate.

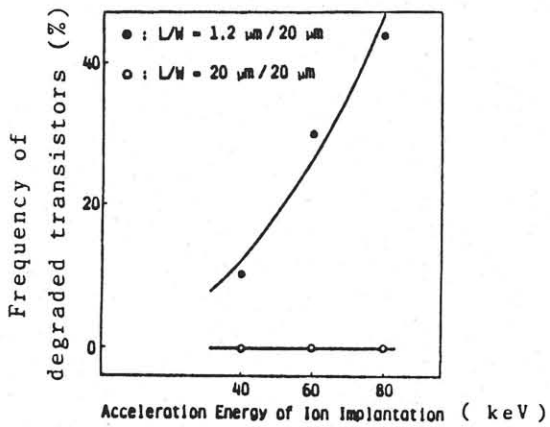

Fig.6 Frequency of degraded ($|(V_{th}$ shift)$|>0.1V$) transistors vs. acceleration energy of ion implantation.

3. Influence of channeling on VLSI circuits

The dynamic RAM sense amplifier is the circuit which requires the highest sensitivity in VLSI circuits. Even if a little degradation of V_{th} in the component transistor takes place, the circuit sensitivity changes and error operation of the circuit is brought about. So we investigated the influence of MOSFET degradation induced by ion channeling on the sensitivity of the sense amplifier, using the circuit simulator, SPICE. By the use of the three-dimensional Table-Look-Up model [7] developed in Toshiba, all the degraded transistor characteristics were taken into the circuit simulator. In the inserted figure of Fig.7, Tr.Q_2 is a normal transistor and Tr.Q_1 is a degraded one induced by ion-channeling. The sense amplifier sensitivity, $V_{bit}-V_{\overline{bit}}$, is in proportion to the V_{th} unbalance, δV_{th}, of the transistor pair, as shown in Fig.7. If power supply voltage, V_{cc}= 4V, capacitance ratio, C_B/C_S= 10, and sensitivity margin is 1/10, the sensitivity of the sense amplifier requires 20 mV. In this case,

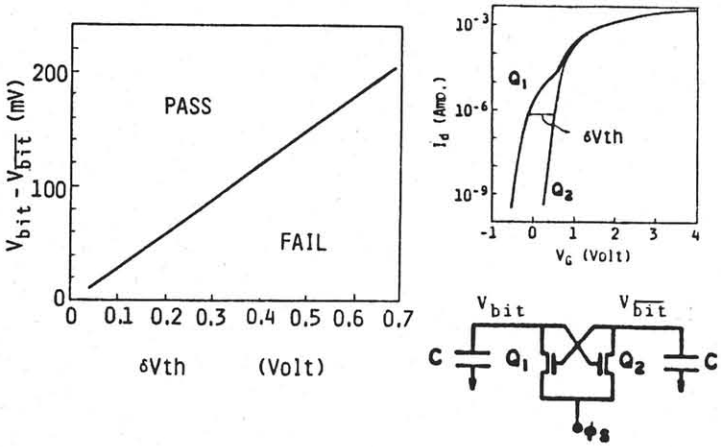

Fig.7 Sense amplifier sensitivity, $V_{bit}-V_{\overline{bit}}$, as a function of V_{th} unbalance between Tr.Q1 and Tr.Q2, δV_{th}.

the maximum permissible unbalance, δV_{th}, is estimated to be 70 mV by Fig.7. We fabricated n-channel 1M bit Dynamic RAM [8] on condition that ion-channeling occurs easily. Figure 8 shows the relation between the error rate of column mode and the degradation frequency of the sense amplifier transistor. The column tends to do error operation with increase in the frequency of degraded transistors. We designed the transistor process of 1M DRAM, based on the relation.

4. Conclusion

We reported the results of investigation on the degradation phenomena of short channel MOSFETs induced by the ion-implantation channeling. The characteristics are as follows.

1) Short channel MOSFETs degrade even in much lower acceleration energy than long channel ones. This phenomenon doesn't always occur in all transistors, but only a few transistors degrade.

2) The degradation is attributed to the hump structure in I_d-V_g characteristics, which is caused by the diffusion spot of n-type impurity due to ion channeling.

3) Short channel MOSFETs are much more sensitive than the long channel ones to the ion channeling.

4) The degradation has strong correlation to the grain size of poly-silicon gate ,and is suppressed by the use of the mean grain size smaller than 0.1 μm when the deposition thickness of poly-silicon is 4000 Å.

We investigated the influence of the MOSFET degradation on the sense amplifier and the DRAM, and estimated the permissible level of the MOSFET degradation.

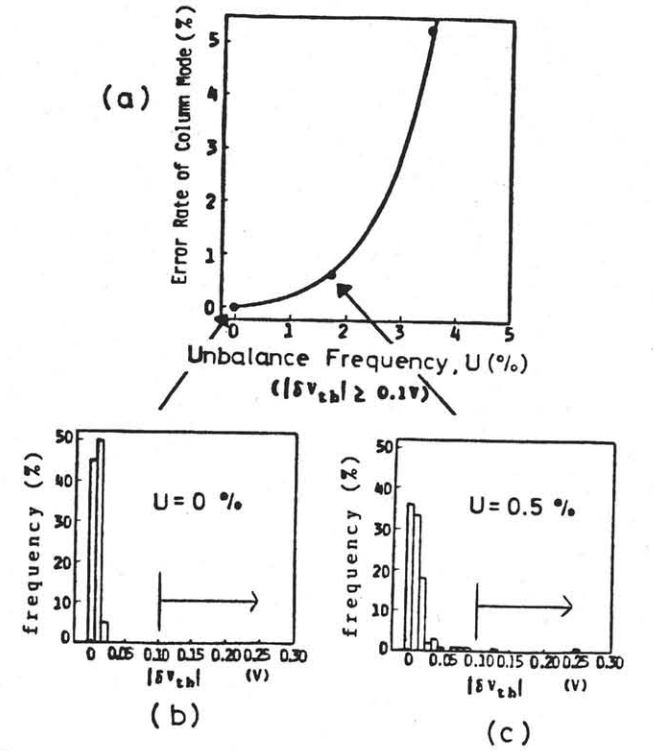

Fig.8 (a) Relation between error rate of column mode in DRAM and unbalance frequency, U, where $|\delta V_{th}|>0.1V$ in sense amplifier transistor pairs, (b),(c): frequency of $|\delta V_{th}|$ at U=0 and 0.5 %,respectively.

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