Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 57-60

P-well/N-well Compatible CMOS Processing for ASIC Applications

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This paper describes p-well/n-well compatible CMOS device structure and processing for ASIC applications, together with a design methodology and a scaling scenario. Process optimization has been carried out with careful adjustment of impurity profiles. Practically equivalent characteristics have been successfully realized in both processes in regard to transistor characteristics, speed performance and latch-up immunity. Scaling philosophy has also been established and its properties are demonstrated.

§1. INTRODUCTION

In the area of Application Specific Integrated Circuits (ASICs), a wide variety of circuit and device combinations is required for various applications. In order to meet the requirement quickly with high performance, it is the best way to prepare many kinds of functional cell library in advance, and combine them to develop new products utilizing automated design tools. However in general, each cell is designed under an optimized condition at the development stage, thus causes several different device architecture as a whole library. Therefore, it is not realistic to integrate them directly on the same LSI chip. On the other hand, the rapid growth in scaled CMOS technology makes it too difficult to prepare all kinds of fundamental cells for each device generation without spending a lot of time and efforts. What is worse, it would prevent implementation of the latest leading edge technology.

In order to settle this problem, a p-well/n-well compatible device architecture has been established so that any circuits originally designed on a p- or n-well process can also be realized together on the same chip. Besides, introducing scaling methodology, the products in any generations based upon the common design rules throughout consecutive generations, can be registered and utilized as common data-base for the function cell without redesigning.

In this paper, an approach on device architecture and design methodology is discussed in detail. Application to 1.5 μm CMOS devices are also described based upon the experimental results.

§2. DEVICE ARCHITECTURE

P-well process has long been the standard CMOS technology which offers better balance on its device performance between NMOS and PMOS in static logic circuits. The difference of the p- and n-well devices, however, have been diminishing after 2 μm device generations, since the impurity profile in channel regions dominates the active device characteristics[1]. The advantage and disadvantage of these two distinct well configurations has widely been discussed from the viewpoint of materials, process controllability, reliability, performance, circuit design, applications and the future prospect[2][3][4]. But there seems to exist no clear conclusion. Considering the widespread applications in ASIC field, it is increasingly effective and important to enable to switch the substrate doping polarity without paying any attention to its influence.

Twin-tub technology is one of the solutions. Advancing to submicron devices, this approach gives wider flexibility of the device design in controlling threshold voltage of parasitic field

transistors and latch-up immunity. However, at the same time, that results in higher junction capacitance and excessive process steps. In terms of lower junction capacitance and fewer process steps, it is actually a better approach in 1.5 μm device generation to use deep implant for punch through prevention and realize fully compatible p-well/n-well structure by adjusting impurity profiles. In order to achieve full compatibility, key parameters were categorized into three, i.e. active, passive and reliability related issues, then device architecture and process integrations have been carried out. Process optimization has been performed with careful adjustment of substrate/well structures and impurity profiles both in active and passive regions. Fig. 1 shows the channel impurity profile in the n- and p-channel devices by SUPREM.

N-channel devices have been fabricated using double diffused drain structures to improve the hot-electron-induced degradation. P-channel devices have been realized using BF_2 implant in the source-drain area to achieve shallow junction depth. The 1.5μm p-well/n-well compatible CMOS structure has been successfully developed where 0.9μm effective channel length for both PMOS and NMOS are provided with an advanced coplanar isolation, low temperature reflow, tapered contact etching and planalized double metal technology.

§3. DEVICE PERFORMANCE

Table 1 shows the comparison of transistor characteristics fabricated with a p- and n-well technology. The saturation current ($V_{DS}=V_{GS}=5$ volts, $L_{poly}=1.5\mu m$), body effect and subthreshold slope are fairly comparable in both processes. Practically identical device performance has been obtained with careful adjustment of the impurity profiles in channel regions. Parasitic field transistors also have the similar characteristics, while the balance of the junction capacitances in both processes is slightly different. Nevertheless, the difference is only effective to speed performance on NMOS majority circuits such as n-channel ROMs and domino circuits.

In order to verify the device performance at real LSI, speed performance for various different logic gates with several different capacitive loads have been evaluated using testers. Fig. 2 shows the propagation delay of a 2-input NAND gate as a function of the inverse of transistor driving current. This parameter can indicate speed characteristics very effectively, especially when the device size such as poly gate length has some tolerance. Speed performance of the basic cells in real LSI circuits has been proven to be fully comparable in both structures.

It was found that there is no practical difference in latch-up immunity of a p- and n-well process through intensive evaluation using various test structures. In both processes, input and output stage latch-up could be effectively prevented by layout consideration and appropriate designs of interface circuits. Moreover, some part of the triggering current introduced to the drain of the output buffers flows into the power supply lines through the parasitic lateral bipolars formed among drain, substrate/well and source. In this way, the substrate current can be reduced drastically. On the other hand, it is relatively difficult to find out where the actual internal latch-up is induced on the chip. With reduction of device geometry in bulk CMOS structures, impact ionization in the higher electric field near the drain results in more substantial substrate current and degrades the latch-up susceptibility. Therefore, the internal latch-up becomes a real issue in developing scaled CMOS devices.

N-channel devices provide much higher substrate current, which can be sunk rather easily when they sit in the substrate. Therefore, the n-well process which allows n-channel devices to stay directly in the substrate region is generally considered to be preferable. The substrate current, however, is produced transitionally by a switching transistor. The pnpn structure also has a time constant proportional to the two base transient times and the spread CR time constant in the well and the substrate. Latch-up immunity is quite improved in the actual circuit environments and even more with a circuit cleverness. Inverter gates with the most adverse layout conditions were designed to characterize the maximum operating voltage dependence on the input signal transient time. Fig. 3 shows the result of the evaluation. Below

100ns region, p- and n-well start to merge. With tight biasing of the well and the substrate, the p-well devices also can work up to the near maximum operating voltage of a transistor as the n-well devices. Design guideline to prevent the internal and external latch-up was determined, effectively.

§4. SCALING SCENARIO

Scaling scenario assumes two major premises. One is that a CMOS circuit has high design margin and high scalability. In this sense, the clocked CMOS circuit is more preferable to the transmission gate circuits which are easily influenced by body effects. The other is that in a long view the progress of each technology required in scaled CMOS is accomplised in a well-balanced way. Fig. 4 shows the actual trend and the future prospect of the critical dimension of the pattern pitch as a function of device generation. Though lithography, process and device technology have progressed at their own pace, the process limitation is scaled down almost linearly.

Scaling is carried out as following.

(Drawing + Partial Resize) * Shrink + Resize

"Shrink" scales pitch downwards proportionally. "Resize" divides the size of the pitch into line and space at any ratio. Such an unproportional scaling procedure without changing the poly gate length can be realized to a certain extent. Since the resize value of the poly layer is usually fixed for maintaining desirable gate length, poly overlaps around contact may run short. In that case, the contact on poly should be extracted and oversized, and then add the data to the poly layer. With introduction of "Partial Resize" like this, fine tuning on geometry can still be carried out. The above mentioned procedure can be accomplished by the combination of fundamental functions as extraction, composition, oversize, undersize and shrink so that it can easily be supported by a CAD system.

Fig. 5 shows the scaling progress of the CMOS MPU designed in 1982 and their features. Speed performance as well as chip size has improved by adopting advanced device generations. Fig. 6 shows a printer controller realized in a 2 μm CMOS device by Super Integration architecture. The cells were designed in different generations and integrated on the same chip. Scaling methodology thus enables any product in any generation to maintain common data-base throughout consecutive device generations. Moreover, integrating the cells on scaled CMOS devices can offer highest performance at that moment and satisfy the various requirement in ASICs very flexibly.

§5. CONCLUSION

A fully design compatible p-well/n-well CMOS technology has been realized with a consistent process optimization. Scaling scenario has also been established and proved to be a very effective approach for various applications in the field of ASICs.

ACKNOWLEDGMENTS

The authors are grateful to S. Kohyama, Y. Suzuki, M. Mukai and M. Ishibashi for their supports and encouragements throughout this work.

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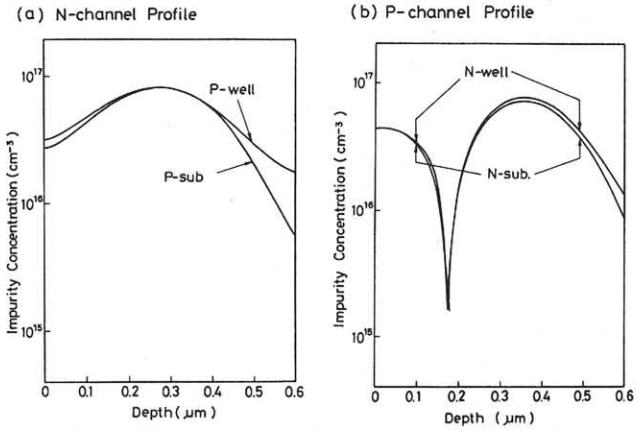


Fig. 1 Profile of impurity concentration in the channel region of a n-channel and a p-channel transistor as simulated by SUPREM

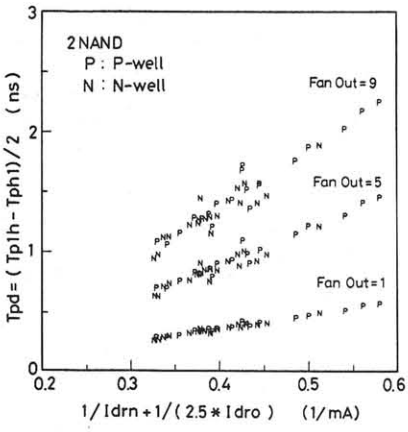


Fig. 2 Gate delay characteristics for a 2-input NAND

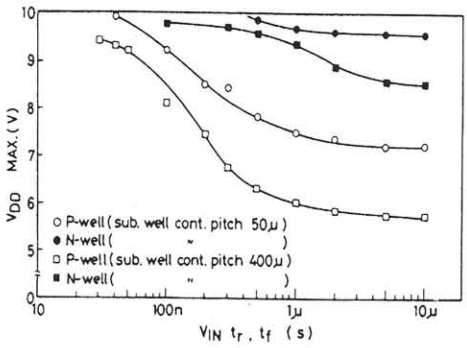


Fig. 3 Maximum operating voltage vs. input signal transient time

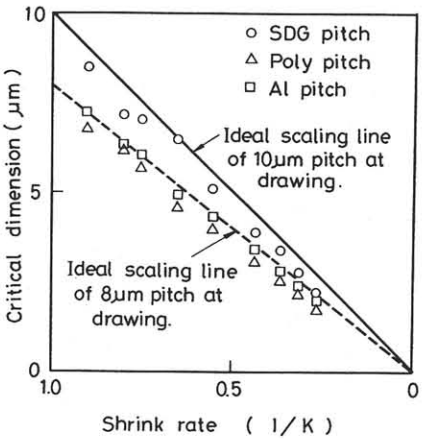
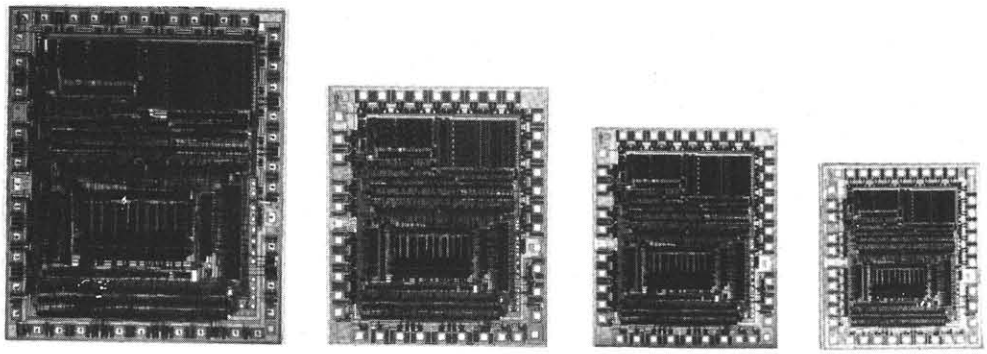


Fig. 4 The trend of scaling technology



Shrink rate (1/K)	x 0.9	x 0.65	x 0.55	x 0.44
Device generation	3.5 μm	2.5 μm	2.0 μm	1.5 μm
Chip size	6.84 x 5.67 mm	5.43 x 4.51 mm	4.62 x 3.83 mm	3.92 x 3.30 mm
Maximum operating frequency	4 MHz	4 MHz	6 MHz	8 MHz
Year	1982	1983	1984	1985

Fig. 5 Scaling progress of CMOS MPU

Table 1 Comparison of p-well and n-well devices

Item	P-well	N-well	Unit	Comment
Transistor				
---N-channel (DDD)--- Saturation Current	220	220	μA/μm	VD=VG = 5 Volts L gate = 1.5 μm
Body Effect (γ)	1.0	1.03	$\sqrt{V}$	
Subthreshold Slope	0.11	0.1	Volt /dec.	
---P-channel--- Saturation Current	90	90	μA/μm	VD = VG = -5 Volts L gate = 1.5 μm
Body Effect (γ)	0.74	0.77	$\sqrt{V}$	
Subthreshold Slope	0.09	0.085	Volt /dec.	

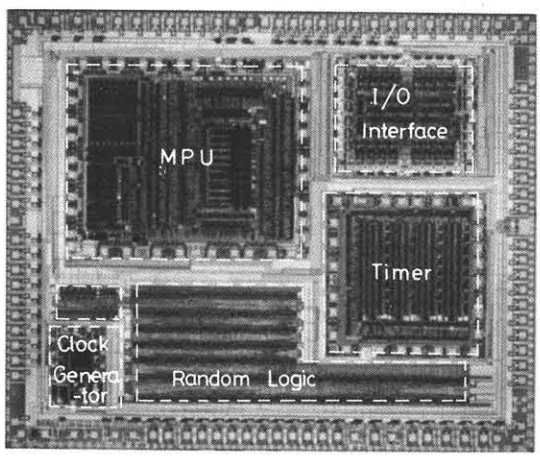


Fig. 6 Printer controller realized by SI architecture
Chip size 7.4 mm x 8.94 mm
Process 2.0 μm P-well double metal
Cell developed year
MPU(1982), I/O Interface (1982), Timer (1983), Clock Generator (1983), Random Logic (1985)