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Advanced OSELO Isolation with Shallow Grooves for Three-quarter Micron ULSIs

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A three-quarter micron isolation process which is compatible with the LOCOS process is described. This new isolation utilizes an advanced offset local oxidation (OSELOII) process with shallow grooves. The OSELOII process is characterized by (1) a size-shifted thin Si_3N_4 mask identical to that used in the original OSELO process[1] for formation of bird's-beak-free oxidation, (2) the formation of shallow self-aligned Si grooves, and (3) a two-step boron implantation which eliminates leakage current along the isolation sidewall.

Introduction

As device dimensions are scaled down to the submicron range, isolation technology becomes one of the most important subjects in order to produce ULSIs. For realization of submicron isolation, (1) reduction in the local oxidation bird's beak and (2) increase in effective isolation length, are necessary.

Several isolation technologies[1)-6)] have been proposed in order to fulfill the above mentioned conditions. However, it was difficult to apply them to submicron ULSI fabrication because of process difficulties such as formation of a sidewall slope in the SWAMI type isolation[3)], removing of "white ribbon" due directly to nitridation of silicon dioxide or silicon substrate in the SILO type isolation[2)4)], and impurity doping on the sidewall of the silicon groove in trench type isolation[5)6)].

This paper proposes a new isolation process OSELOII, which is compatible with the LOCOS process. The active MOS transistors and parasitic MOS transistors using OSELOII isolation are characterized.

OSELOII isolation technology has achieved both a reduction in the local oxidation bird's beak and an increase in effective isolation length.

PROCESS

The OSELOII process is similar to the LOCOS process shown in Fig.1 (a)-(e). First, Si_3N_4 film for selective field oxidation is deposited on a thin pad of SiO_2 and patterned (a). Next, thin Si_3N_4 film for bird's-beak-free selective oxidation and SiO_2 film are deposited by chemical vapor deposition (b). Sidewall spacers are, then, formed using reactive ion etching and 0.2um-deep Si grooves are formed by dry etching (c). Next, the SiO_2 film on the Si_3N_4 layer is removed (d), and finally thick oxide is formed over the field region using selective oxidation (e). Using two-step implantation, boron doped regions are formed under the field oxide as a channel-stopper. The first implantation is made following process step (a) to avoid causing an inversion in the sidewall of the shallow grooves. The second implantation is made following process step (c) to avoid causing an inversion in the bottom of the shallow grooves.

The final cross sectional SEM photograph of the OSELOII isolation is shown in Fig.2 compared with the previous OSELO isolation photograph, where the increased effective isolation length in the OSELOII structure is clearly shown.

ELECTRICAL CHARACTERISTICS

Threshold voltage V_{thp} of parasitic field MOS transistors with 0.7um-wide designed isolation length and threshold voltage deviation ΔV_{th} of

narrow channel active MOS transistors are shown in Fig.3 as a function of the surface boron (SB) dose. Here, ΔV_{th} is equal to V_{th}(0.8um-wide designed channel width) - V_{th}(5um-wide designed channel width). Obviously, V_{thp} is independent of the SB dose; on the other hand, ΔV_{th} is almost linear to the SB dose. V_{thp} and ΔV_{th} dependences on the bottom boron (BB) dose are shown in Fig.4. V_{thp} increases as a function of the BB dose, whereas only ΔV_{th} has a weak dependence on the BB dose. Therefore, V_{thp} and ΔV_{th} can be controlled by the BB dose and the SB dose, independently, which allows more freedom in designing process parameters. $2*10^{13}cm^{-2}$ and $3.5*10^{13}cm^{-2}$ are determined as an optimized SB dose and an optimized BB dose, respectively, in order to minimize narrow channel effects of the active transistors and minimize short channel effects of the parasitic field MOS transistors.

In the optimized OSELOII structure, the leakage current at the sidewall of isolation did not appear as shown in Fig.5, as neither did the hump[7] characteristics due to the sidewall region's inversion.

Fig.6 shows dependence of the normalized transconductance $g_m/g_m(5)$ on the designed channel width, where $g_m(5)$ is transconductance of an active transistor with effective 5um-wide channel width. Since g_m is proportional to the effective channel width, an extrapolated value of the measured points to the x-axis gives an electrical channel width shrinkage ΔW from the designed channel width. As can be seen from Fig.6, ΔW of the LOCOS is 0.6um, whereas that of OSELO and OSELOII is 0.2um. This shows that a large improvement in the channel width narrowing can be obtained by the OSELOII structure. Furthermore, the bird's-beak-free structure in OSELOII exhibits a much smaller increase in V_{th} due to the narrow channel effect than the LOCOS structure as shown in Fig.7. The threshold voltage of the LOCOS transistor drastically increases in the region of the channel width below 1um due to the large ΔW. On the other hand, in the OSELOII transistor, the narrow channel effect is reduced similarly to the previous OSELO's.

Consequently, by using the OSELOII structure, the current drivability of the narrow channel active MOS transistor can be significantly improved compared to that of the LOCOS structure as shown in Fig.8. In the OSELOII transistor with a three-quarter micron channel width, more than 60% larger drain current flows than that in the LOCOS transistor with the same design dimensions.

The short channel effects of parasitic MOS transistors are shown in Fig.9. The OSELOII structure features larger V_{thp} values and less short channel effects than the LOCOS and OSELO structures because the shallow grooves of the OSELOII structure increases the effective isolation length. Moreover, OSELOII provides unexpected improvement in self-feedback in short channels. That is, as the isolation length becomes less than 1um, the bird's heads at both edges of the isolation begin to approach each other and merge, thus increasing the effective field oxide thickness as shown in the inset of Fig.9. Moreover, because of its deep isolation depth and its sharp bottom edge shape, the electrical field strength from the aluminum gate electrode at the isolation bottom edge is reduced. Therefore, V_{thp} in the short channel region becomes large enough to compensate for the lowering of V_{thp} due to the short channel effect.

Fig.10 shows backward current-voltage characteristics of n^+-p junction diodes with a $200*200um^2$ area. In the small voltage region, the reverse leakage current of the OSELOII structure is several times larger than that of the LOCOS structure. This is considered to be due to the mechanical stress at the edge region of the OSELOII structure. Therefore, the field oxide thickness and the oxidation condition should be optimized to decrease such stress.

Perspective of the submicron isolation technology is shown in Fig.11, where the LOCOS, OSELO and OSELOII isolation technologies are compared. In the LOCOS structure, the minimum isolation size is limited by the narrow channel effect of the active MOS transistors, which results in a minimum isolation length of about 1.1um. In the original OSELO structure, the minimum isolation size is not limited by the narrow channel effect but is limited by the short channel effect of the parasitic MOS transistors. Therefore, OSELO is capable of producing 0.9um

isolation. Since the OSELOII structure shows superior short channel effects of parasitic MOS transistors and small narrow channel effects of active MOS transistors, OSELOII is suitable for use in three-quarter micron isolation.

SUMMARY

A new isolation technology, OSELOII, has been developed. This isolation process features: a LOCOS compatible process, an improvement in current drivability for narrow channel devices, and large threshold voltage of the parasitic field MOS transistors in the submicron range. These results demonstrate that the OSELOII isolation process is promising for three-quarter micron ULSI production.

ACKNOWLEDGMENT

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5) T.Shibata et al., ibid., 1983, p.27

6) N.Kasai et al., ibid., 1985, p.419

7) K.Kurosawa et al., ibid., 1981, p.384

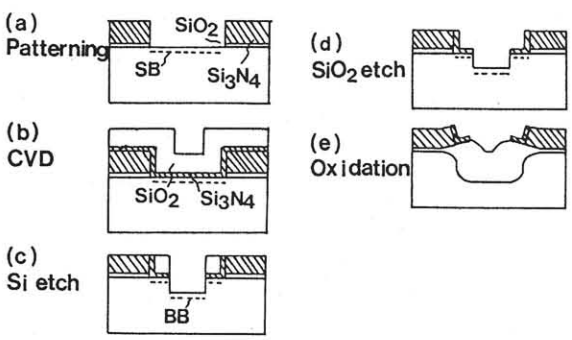

Fig.1 Fabrication process steps in OSELOII. SB: surface boron doped region. BB: bottom boron doped region.

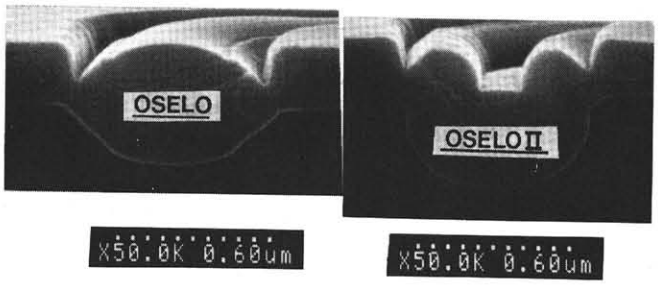

Fig.2 Cross sectional views of OSELO and OSELOII obtained by SEM.

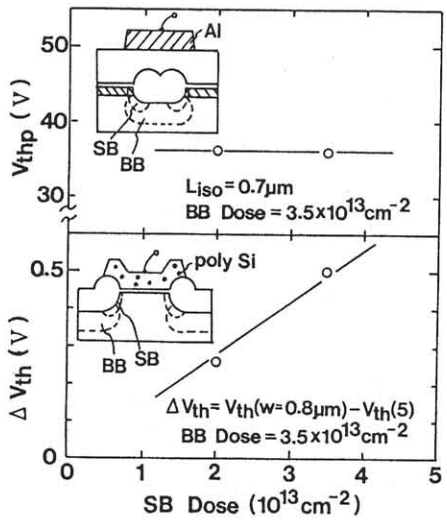

Fig.3 V_{thp} and ΔV_{th} dependence on SB dose. V_{thp} is the threshold voltage of a parasitic field MOS transistor with 0.7um-wide designed isolation length and ΔV_{th} is equal to the deviation of the narrow channel (W=0.8um) threshold voltage from that of the wide channel (W=5um).

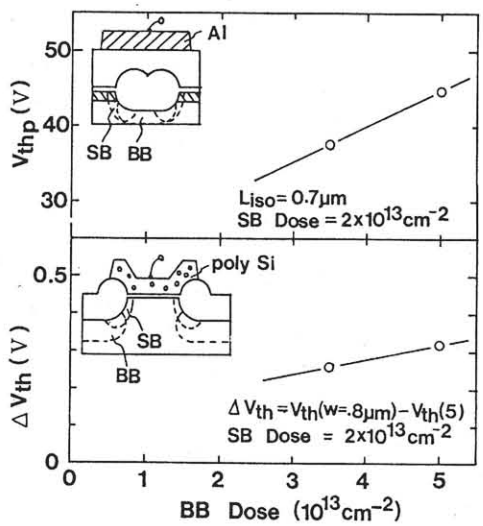

Fig.4 V_{thp} and ΔV_{th} dependence on BB dose.

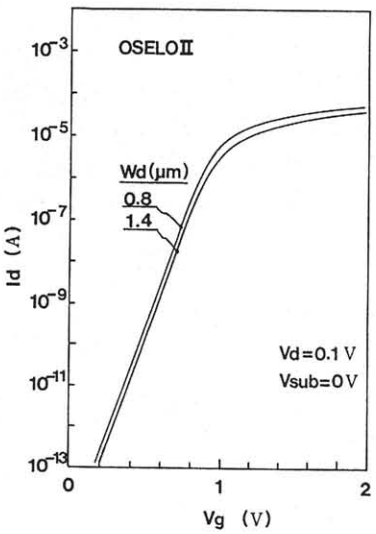

Fig.5 Subthreshold characteristics of optimized active OSELOII MOS transistors.

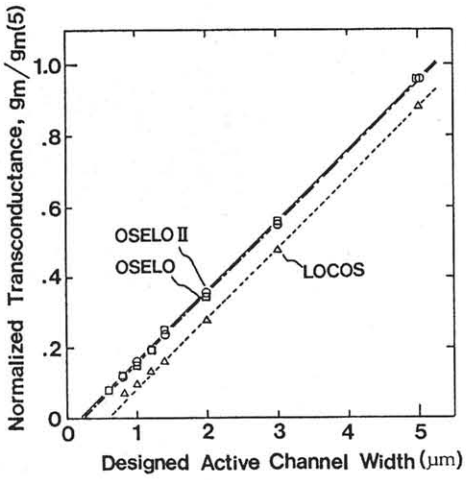

Fig.6 Transconductance of OSELOII, OSELO and LOCOS as a function of designed channel width.

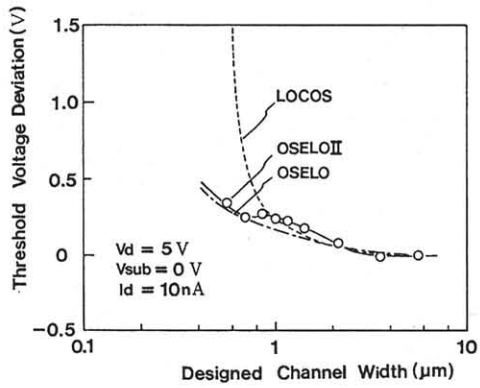

Fig.7 Threshold voltage of LOCOS, OSELO and OSELOII as a function of designed channel width showing the narrow channel effects.

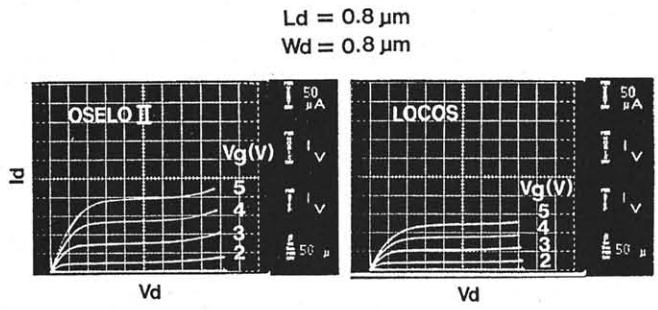

Fig.8 Drain current vs. voltage characteristics of OSELOII and LOCOS transistors with a 0.8um designed channel width and a 0.8um designed channel length.

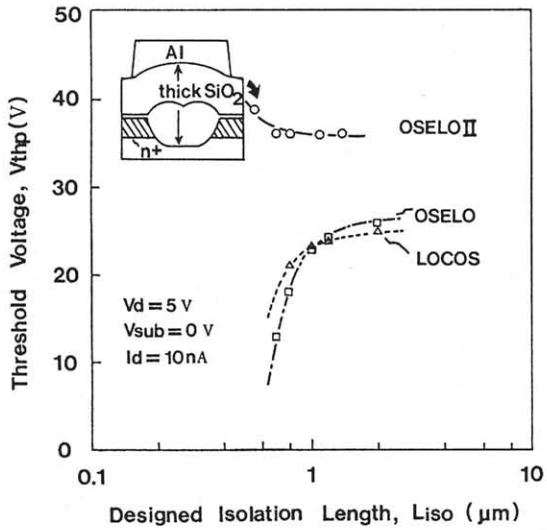

Fig.9 Threshold voltage of parasitic field MOS transistors fabricated by using LOCOS, OSELO and OSELOII technology as a function of isolation length (L_{iso}).

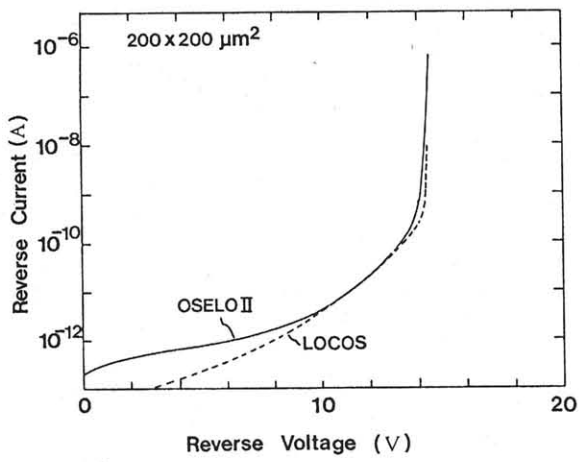

Fig.10 Backward current-voltage characteristics of n^+-p junction diodes.

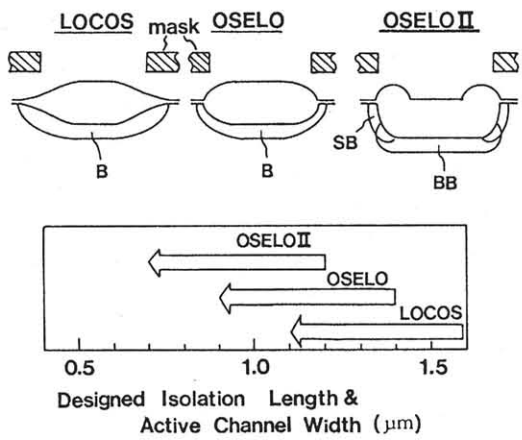

Fig.11 Perspective on submicron isolation technology showing the minimum isolation length of LOCOS, OSELO and OSELOII structures. SB: surface boron doped region. BB: bottom boron doped region.