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An Analog BIMOS Technology

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A BIMOS technology with a novel and compact isolation structure is discussed. The structure consists of self-aligned p+ buried layers between the n+ buried layers and of a shallow boron implant between the n-wells. This causes a dependence of both MOS and bipolar parameters on epilayer thickness. The optimization of the epilayer thickness for analog applications is discussed and a deflection control circuit for computer controlled TV is presented as an illustration.

1. Introduction

A merged Bipolar-CMOS process (BIMOS) for analog digital circuits requires a rather different optimization from that for a pure digital application. For precision current sources a careful compromise of the ft and Early voltage is required and in fact all AC and DC parameters of both npn and pnp and MOS devices have to be tuned carefully. In this paper a novel and compact isolation structure is presented in a 2.0 µm BIMOS technology. Some trade-offs between important parameters are discussed and a deflection control circuit for computer controlled TV is presented as a typical example.

2. Isolation structure

To obtain a high packing density and to avoid latch-up or punchthrough, self-aligned p+ buried layers are applied between two adjacent n+ buried layers: in addition to the conventional function of the n+ layers in the bipolar devices both n+ and p+ layers reduce the latch-up sensitivity of the CMOS. The n+ buried layers contain both antimony and phosphorus (25 Ohms/sq.), the p+ buried layers are boron doped (200 Ohms/sq.). By using identical implantation doses for boron and phosphorus the lateral displacement of the p-n junction during subsequent diffusion steps is minimized.

After the buried layer procedure a p-type epitaxial layer is grown and after an n-well implant a well drive serves to connect the n-wells top to bottom. The concentration in the surface layers is determined by the implantation dose in the n-well and by the epilayer resistivity in the p-well. After the completion of the wells, standard CMOS processing is applied using phosphorus doped polysilicon gates and double layer metallization. A collector plug diffusion and a dedicated base implant are used to obtain an adequate npn performance. In the p-type isolation areas between adjacent bipolar devices the shallow p-type source and drain implant is used to obtain a considerable reduction of the isolation width.

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Fig. 1 shows the simulated p-n junction and the extension of the depletion layers at a reverse bias of 18V. The net n-well to n-well distance is 4 µm. Fig. 2 shows the corresponding situation if the shallow p+ area is omitted: the n-well to n-well distance should be at least 6.5 µm. Fig. 3 shows the situation where the buried p+ layer is omitted: the n-well to n-well distance should be at least 9 µm to prevent punchthrough. Finally fig. 4 shows an optical micrograph of a cross-section of the isolation structure: the anisotropic structure of the isolation is clearly visible.

3. Epilayer thickness

The presence of both p+ and n+ buried layers causes the device parameters for both MOS and bipolar devices to be dependent on the epilayer thickness.

The doping profile in the collector of the npn transistor is the aggregate of the phosphorus well diffusion from the surface and of the antimony and phosphorus updiffusions from the buried layers. In practice an initial epilayer thickness of 5.25 µm corresponds to a final concentration of 1E17 cm^{-3} at a depth of 3.3 µm. The dependence of the maximum cut-off frequency of the npn transistors on the epilayer thickness is shown in fig. 5. In all cases the DC current gain is 200 and the emitter-collector breakdown voltage is at least 12V, except for the epilayer of 4.25 µm. The corresponding data on Early voltage (fig. 5) indicate that an Early voltage above 50V can only be obtained at an epilayer thickness of at least 5.0 µm, thereby limiting the maximum ft to 4.25 GHz.

The base of the lateral pnp transistors is covered with field oxide. The dependence of the current gain on epilayer thickness is also

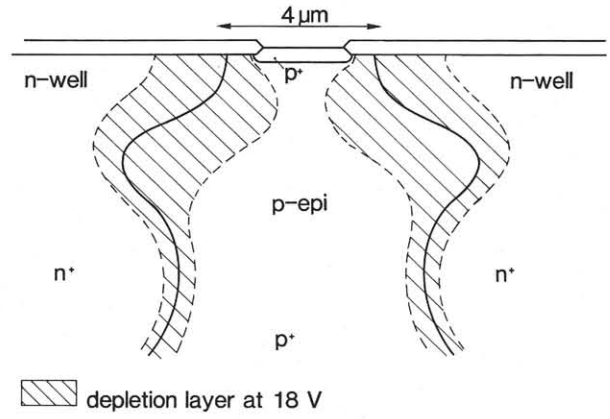

Fig. 1. Simulation of the isolation structure.

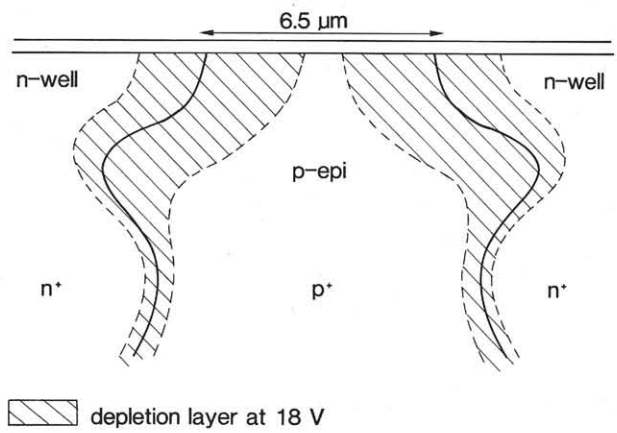

Fig. 2. Simulation of the isolation structure without shallow p+ diffusion.

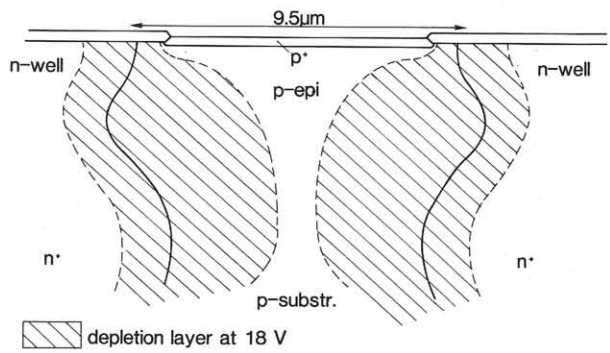

Fig. 3. Simulation of the isolation structure without the buried p+ layer.

plotted in fig. 5. The basewidth is always 3.5 µm.

The effect of the epilayer thickness on the body effect of the MOS devices can be seen in fig. 6. The k-factor of the n-channel MOS devices is higher than in a pure CMOS process (which has k=0.33 V**1/2), and it shows a significant dependence on the epilayer thickness. The k-factor for the p-channel transistors increases less quickly than for the n-channel devices, and is not much higher than in a pure CMOS process (which has k=0.70 V**1/2). The standard epilayer thickness was chosen to be 5.25 µm and the corresponding device parameters are listed in table I.

npn	hfe	200	NMOS	Vt	0.75 V
	ft	4.2 GHz		k	0.44 V**1/2
	V_{early}	75 V		beta	50 µA/V2
	BV_{ceo}	16 V			
pnp	hfe	100	PMOS	Vt	-0.80 V
	ft	30 MHz		k	0.76 V**1/2
	V_{early}	25 V		beta	17 µA/V2
	BV_{ceo}	20 V			

Table I. Device parameters for MOS and bipolar.

4. Deflection control circuit

Fig. 7 shows a micrograph of a typical BIMOS circuit: a deflection control circuit for colour TV sets and monitors. The circuit comprises an analog geometry processor using translinear circuit techniques. It drives the vertical deflection and East-West raster correction stages of the TV set.
The waveforms at each of the two outputs can independently be controlled by in total ten parameters. The values of these parameters are sent to the circuit via the serial I2C bus transceiver,

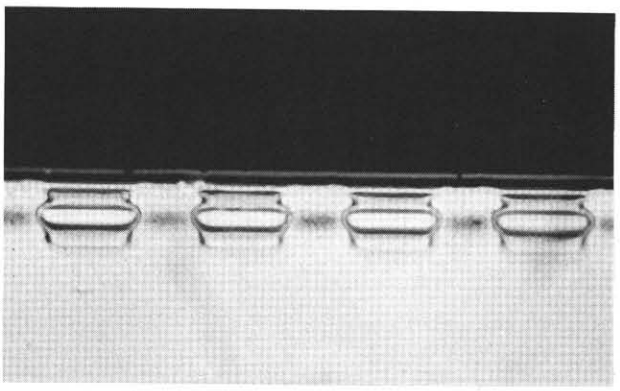

Fig. 4. Cross-sectional view of the isolation structure.

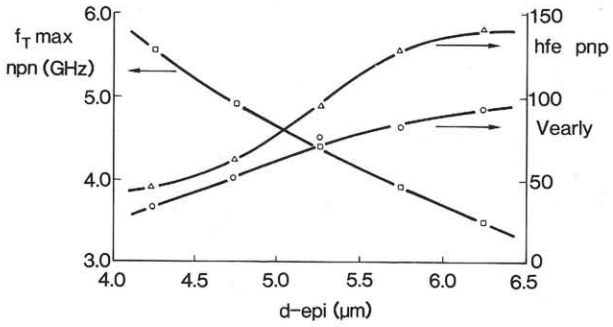

Fig. 5. Dependence of bipolar device parameters on epilayer thickness.

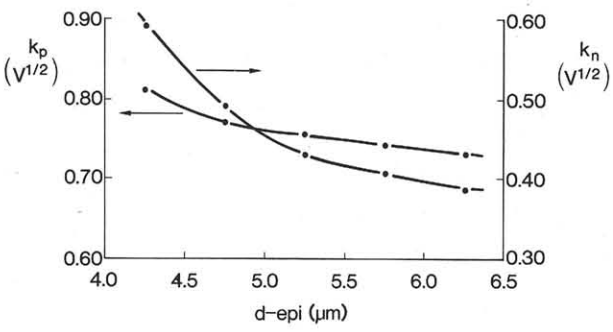

Fig. 6. Dependence of MOS device parameters on epilayer thickness.

which is designed in CMOS. Subsequently twelve 6-bit Digital-Analog converters are used to translate the twelve digital words into analog signals. These D/A converters contain both MOS and bipolar devices. Ten words are used for the internal processor and two are externally available via two buffers. The analog processor is a full bipolar circuit. The circuit is fully compatible with our Computer Controlled TeleVision concept (CCTV).

The same circuit is also available in an old full bipolar technology with 4 µm design rules. The minimum transistor area in the 2.0 µm BIMOS process is about 4 times smaller than in the 4 µm bipolar technology: in practice the area reduction in the analog processor part is a factor 3 using a coarse design grid.

The CMOS layout of the I2C bus was designed using an automated placing and routing program: compared with the original handcrafted I2L layout, the area reduction factor is about 1.8. This can be improved to a factor of 2 using manual wiring of the standard logic cells.

The twelve D-A converters were designed with a mixture of MOS and bipolar devices. The reference current sources were full bipolar for optimal matching properties. The switches and latches were designed in a mixture of static CMOS and transfer logic, while data transfer gates and the quasi-scantest logic were interlaced with the databus interconnect. With this kind of mixed structures a factor 5 area reduction was achieved.

The total chip size was reduced from 22.7 mm^2 in the old technology to 8.8 mm^2 in the BIMOS chip shown in fig. 7. It can be further reduced to 7.8 mm^2 using manually routed CMOS logic. This represents a reduction of almost a factor 3. Due to the high cut off frequency of the npn transistors all bias currents were reduced with a factor 2 whereas the CMOS logic consumes less current than the original I2L. This gives an overall reduction in dissipation of about a factor 3.

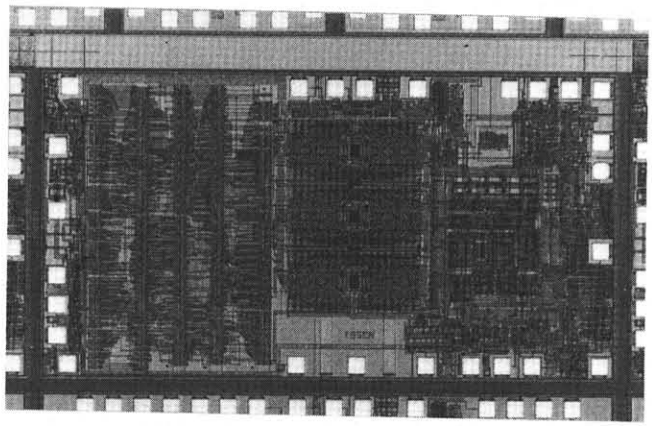

Fig. 7. Deflection control circuit.

Especially the experience with the D/A converters has shown that an inherent reduction in chip size can be achieved with merged bipolar-CMOS technology. Future efforts will be directed towards the design of mixed bipolar-CMOS macrocells for analog applications.