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Normally-Off MOS FETs Using Ultra Thin SOI Structured Si Film

Fumitoshi HATORI and Takuo SUGANO

Depertment of Electronic Engineering,University of Tokyo

7-3-1 Hongo,Bunkyo-ku,Tokyo 113,Japan

Normally-off MOS FETs have been built using ultra thin SOI structured Si film whose thickness is about 200Å. A new technique to form gate oxide is proposed here. That is,the Si film is oxidized thermally at low temperature(~800°C)for 30 minutes,and then SiO_2 film is deposited by plasma enhanced chemical vapor deposition. Fabricated devices showed good FET characteristics. The effective electron mobility μ_{eff} is about 2.0 cm^2/Vs,and the threshold voltage V_t is about 9.8V.

1. Introduction

Recent development of VLSI requests reduction of device dimensions,and the gate length of Si MOS FETs will be reduced into sub-micron range. But MOS FETs of conventional structure show so called short channel effects,and so many kinds of new device structures to suppress the short channel effects,have been proposed. As one of them submicron gate MOS FETs on non-doped SOI(Silicon On Insulator) structured Si film,have been proposed by S.D.S.Malhi et al.[1] The device characteristics have been studied in our group using Monte Carlo simulation[2],and it has been concluded that this type of devices are promising as switching device for VLSI of next generation. However,if the gate length is reduced into submicron range,the thickness of the Si film must become several hundred angstrom to suppress punch through current.

In consequence a new technique to form gate oxide on ultra thin SOI structured Si film is required. Here a double layer technique using thermally grown ultra thin SiO_2 film and SiO_2 film deposited by plasma enhanced chemical vapor deposition,PECVD, is proposed,and the feasibility of this technique has been demonstrated by fabricating long channel(20μm) MOS FETs on SOI substrate.

2. Fabrication Procedure

Figure 1 shows fabrication procedure of devices.

(1)The Si films were patterned into square for isolation using reactive ion etching,RIE. The gas used in this process was CF_4.

(2)Gate oxide films were formed on the substrates using a technique which is described in section 3. The thickness of this film is about 600 Å.

(3)Poly Si films for gate were formed on the gate oxide by PECVD using SiH_4(5%)+PH_3(0.05%)+Ar(~95%). The thickness of this film is about 5000 Å.

(4),(5)The gate was formed by patterning poly-Si using RIE.

(6)The source and drain were self-aligned to the gate poly-Si by implanting P^+ at 70 keV. The dose of P^+ was $1x10^{14}cm^{-2}$.

(7)The implanted ions were activated by rapid thermal annealing,RTA.

(8)SiO_2 films for passivation were deposited by PECVD using SiH_4(10%)+Ar(90%) and N_2O.

(9)The contact holes were formed by chemical etching using buffered HF.

(10)The aluminum pads were formed by evaporation.

The dimensions of the fabricated device are

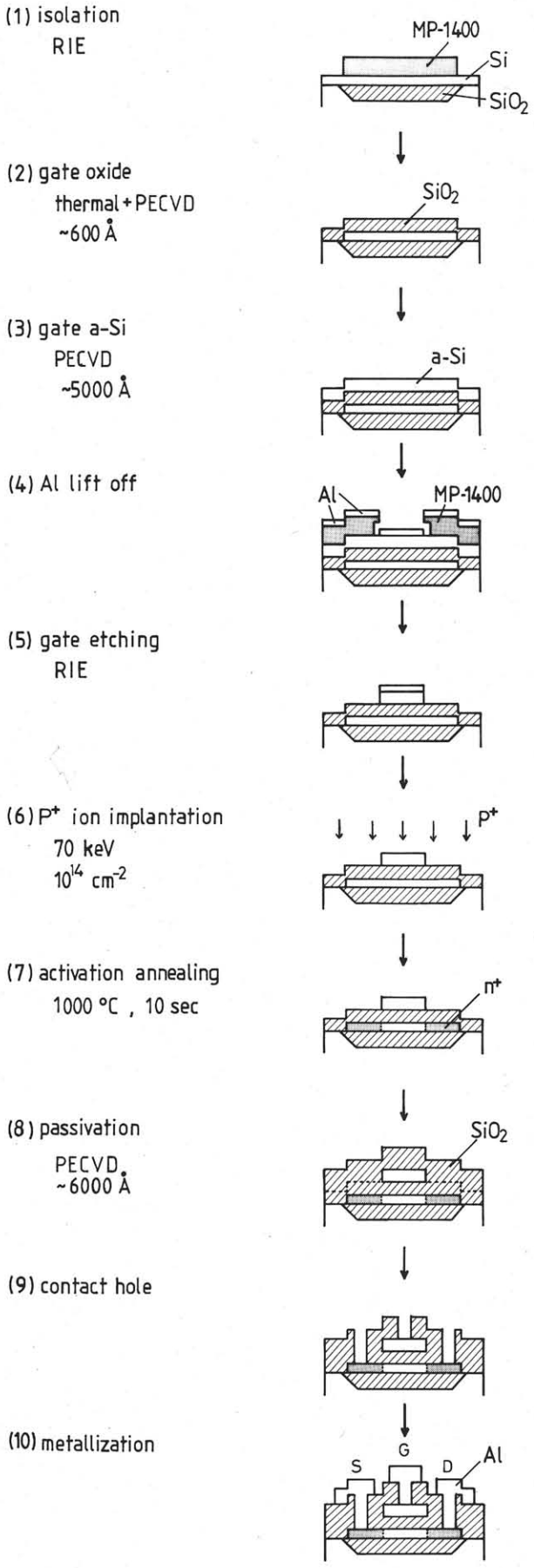

Fig.1 Fabrication procedure

as follows. The gate length is 20 μm,the gate width is 100 μm,the thickness of the gate oxide is 600 Å ,and the thickness of the Si film is 200 Å.

3. Characterization of Si Films and Si-SiO_2 Interface

As SOI structured substrates, ultra thin Si films(~200Å),which were deposited on SiO_2 films by PECVD using SiH_4(90%)+Ar(10%) followed by 7.5 hrs annealing at 1100°C in N_2 ambient with capping SiO_2,was used. The crystalline structure of those Si films was determined by Raman scattering. Figure 2(a) shows Raman scattering signal from as-deposited amorphous Si film,and (b)is from annealed one. This indicates that the Si films have changed from amorphous state to crystalline. The response of the single crystalline Si substrate beneath the SiO_2 film has not eliminated completely. However the response is not observed in Fig.2(a),and therefore the response is believed not to give any significant influence to the result shown in Fig.2(b).

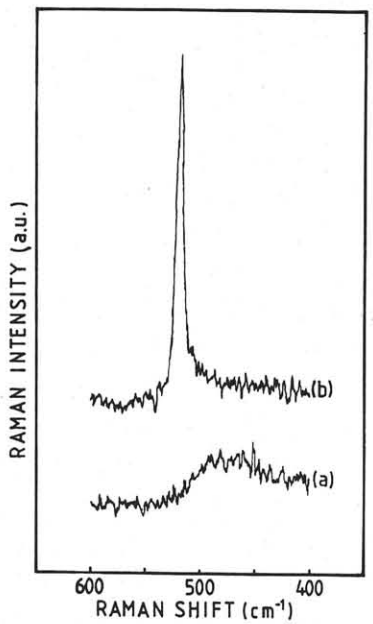

Fig.2 Raman scattering signal from
(a)as-deposited Si film and
(b)annealed Si film

Because of very small thickness of the Si films,the oxidized depth of Si films must be controlled precisely. Therefore Si films were oxidized thermally at low temperature which was about 800°C for 30 minutes (pre-oxidation) and then SiO_2 films were deposited by PECVD. To measure the

interface properties,the double layer oxide were formed on single crystalline Si substrates whose resistivity was 5 Ωcm and of n type. Figure 3 is the density of interface trap states,which was measured by the Terman method.(2) The minimum density of interface trap states is about 2.0×10^{10} $cm^{-2}eV^{-1}$,and this is almost of the same order of magnitude obtained from Si-SiO_2 systems which were formed by thermal oxidation at high temperature.

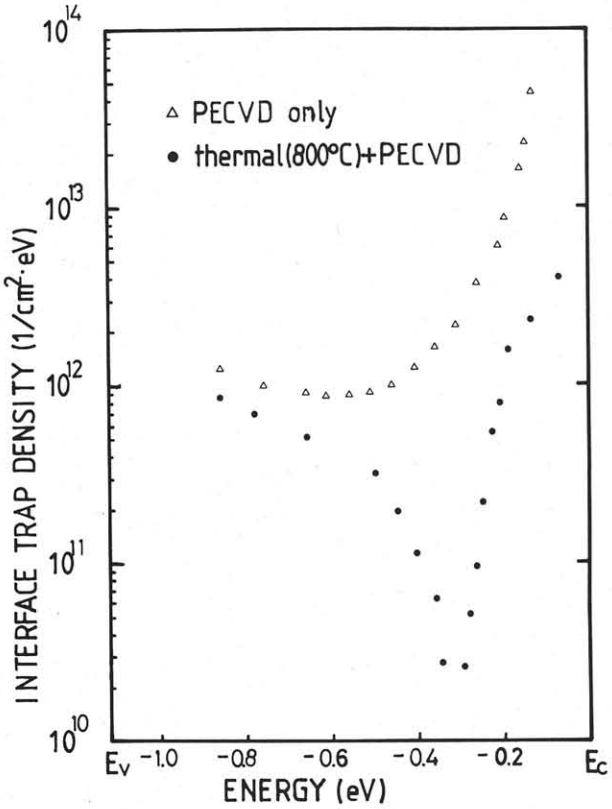

Fig.3 Density of interface trap states between Si substrate and double layer SiO_2

Figure 4 shows flat band voltage versus temperature of pre-oxidation. At 800°C flat band voltage is about the same as obtained from thermal oxidation at high temperature. From these characteristics it is concluded that this double layer SiO_2 film can be used as the gate oxide of MOS FETs,and is useful to fabricate MOS FETs on ultra thin SOI structured Si films.

4. Characteristics of MOS FETs and Discussion

Figure 5 shows the curve tracer characteristics of a SOI MOS FET. The supplied voltage between the source and the drain was about 35 V,and between the source and the gate was 24V. The step of the gate voltage was 2V. The fabricated MOS

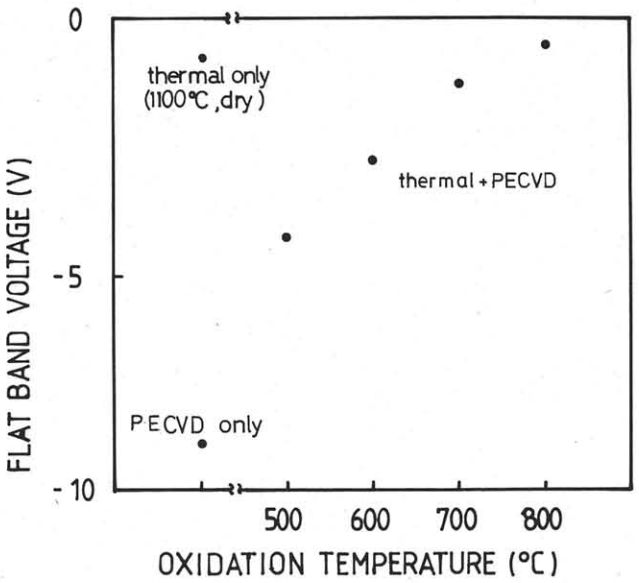

Fig.4 Flat band voltage versus pre-oxidation temperature

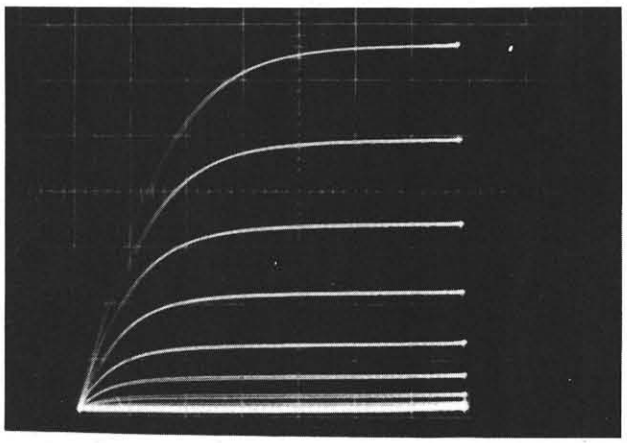

Fig.5 The curve tracer characteristics of a MOS FET

vertical 10 uA/div
horizontal 5 V/div
gate 0-24 V,step 2 V

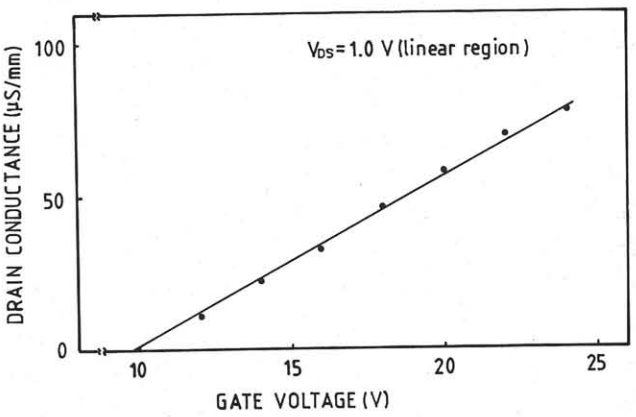

Fig.6 The I_{DS}-V_{GS} curve of the device

FETs are normally-off type devices. There is no hysteresis in this characteristics.

From the linear region of this characteristics(supplied voltage between the source and the drain is 1.0 V),we can obtain g_D-V_{GS} curve,where g_D means the drain-conductance and V_{GS} means the gate voltage.

From this we can obtain the effective electron mobility μ_{eff} and the threshold voltage,using the following equation.

$$g_D \equiv \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=\text{const.}} = \frac{Z}{L} \cdot \mu_{eff} \cdot C_{ox} \cdot (V_{GS} - V_T)$$

where,Z is gate width(here 100 μm)

L is gate length(here 20 μm)

μ_{eff} is effective mobility

C_{OX} is gate capacitance per unit area(here 54 nF/cm^2)

V_{GS} is supplied voltage between the gate and the source

V_{DS} is supplied voltage between the drain and the source

From these it has been found that μ_{eff} is about 2.0cm^2/Vs and the threshold voltage V_t is about 9.8 V. Figure 7 shows I_{DS}-V_{GS} characteristics of this device,when the back gate bias is applied. Here I_{DS},V_{GS} and V_{BG} mean the drain current,the gate voltage and the back gate voltage,respectively. The decrease of the subthreshold leakage current with the increase of the back gate bias indicates that a conducting channel exists at the interface between the Si film and the SiO_2 substrate.

5. Conclusion

Double oxide layer technique using low temperature thermal oxidation and plasma enhanced chemical vapor deposition technique was successfully applied to fabricate normally-off MOS FETs in ultra thin Si film (~200Å) on SiO_2 substrate. The devices showed good FET characteristics such as small saturation voltage and drain conductance,and the electron mobility is about 2.0 cm^2/Vs. It is expected that this technique can be used to fabricate very short channel MOS FETs on SOI substrates.

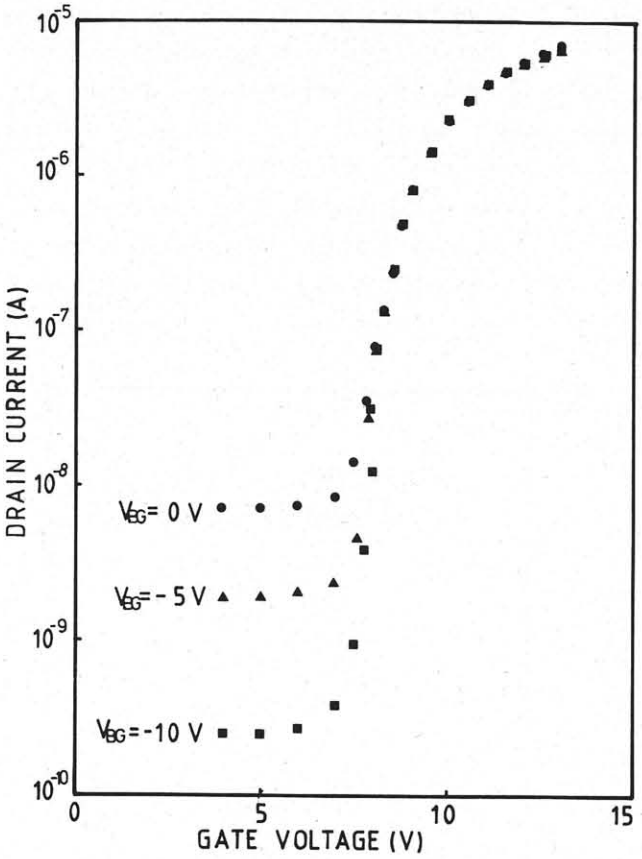

Fig.7 The back gate effect of the device

6. Acknowledgment

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