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Advanced High Mobility Polysilicon Super-thin FilmTransistor (SFT) Using Solid Phase Growth

H.HAYASHI, T.NOGUCHI, T.OHSHIMA, M.NEGISHI, and Y.HAYASHI

Research & development Dept., Semiconductor Group, SONY

4-14-1 Asahi-cho, Atsugi 243, Kanagawa

Recrystallized polysilicon film of 800 A thick through Si^+ implanted amorphization has grains of a maximum size of 5 μm. The carrier mobility and threshold voltage were improved by means of super thin channel thickness. CMOS D-type flip-flop with a maximum frequency of 5 MHz was obtained by using of 7 μm design rule. 19 stage ring oscillator was fabricated. Delay time of 3 nsec and $t_{pd} \cdot Pw$ of 3pJ per stage were observed.

1. Introduction

A thin film transistor on an insulator substrate has a large impact in the region of large size integrated circuits. A super thin film transistor in a large grain polysilicon has been studied, because it has advantages of reproducibility, reliability and producibility. However, electrical characteristics must be improved to use as integrated circuit (IC), for example, carrier mobility and threshold voltage and good gate insulator.

In order to improve the electrical characteristics of polysilicon transistor, a new idea which the thickess of the channel region was reduced to the thickness of inversion layer was proposed, because the potential of a channel was induced effectively by gate voltage even if there was a large number of trap state.[1] In the second idea, the recrystallization on the polysilicon film deposited by LP-CVD (Low Pressure Chemical Vapor Deposition) was proposed to obtain large grains and small amount of trap states.[2,3,4,5]

When a transistor is made on a insulator substrate, there are many advantages, such as low parasitic capacitance, no punch through, no latch up, small isolation area and short process. Silicon on saphire (SOS) has been used to realize the advantage since 1975.[6] Recently, recrystallized silicon on insulator (SOI) has been studied in many reseach center by use of laser beam[7], electron beam[8] and carbon heater[9]. However, it has many disadvantages of low throuput, less controllability and a expensive machine. On the other hand, an amorphous silicon transistor has been studied to realize the integrated circuit at low temperature process in the technological base of amorphous silicon solar cell[10]. But it is impossible to apply high speed electrical circuits because of low carrier mobility. Therefore, a polysilicon film has an attractive candidate for large size and scale ICs in easy fabrication and a suitable electrical properties. In this paper, recrystallization mechanism from amorphous silicon to polysilicon is discussed and MOS transistor characteristics are shown concerning channel dope effect and channel length dependence. The electrical characteristics of CMOS circuits are presented, too.

2. Solid phase recrystallization

A polysilicon film has been deposited at low pressure on a SiO_2 substrate. At that time, average grain size was about a few ten nanometer. In order to enlarge the grain size, the film was amorphized through ion implantation. Si^+ was chosen because of no influence on electrical conductivity. Super thin film has an advantage, because the film was fully amorphized at low energy and small dose implantation of silicon and the probability of nucleation became low. Moreover, many kinds of amorphous states were obtained by changing implantation dose and energy.

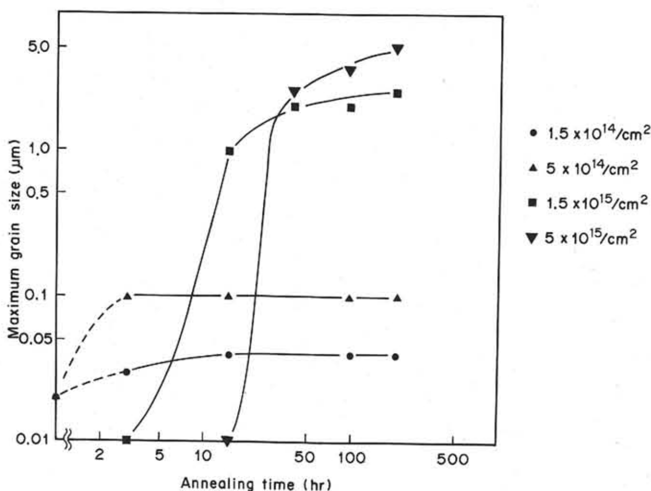


Fig. 1 Maximum grain size vs annealing time at 600°C with Si^+ dose as a parameter

An 800 A thick polysilicon film was deposited at 610°C on a 5 inch SiO_2/Si wafer. Then Si^+ was implanted at 40 keV in the dose range of 1×10^{14} to 5×10^{15} cm^{-2} into the films. Solid phase recrystallization was done in a furnace at 600°C. The films were investigated as a function of the annealing time by TEM (Transmission Electron Microscope). Fig.1 shows the relation of the grain size and the annealing time with Si^+ dose as a parameter. At lower dose than 5×10^{14} cm^{-2}, grain started to grow within an hour because the small crystal in the film remained after implantation. The grain size of about 0.1 μm was observed at this condition. In the dose range more than 5×10^{14} cm^{-2}, the film was entirely amorphized by implantation. Therefore, there was a delay time to grow. After the nucleation of the crystal, a grain grew at the rate of 1 A/sec till the grain reached the neighbor grains. The grain size was determined by the number of nucleus, which increased with the annealing time. Moreover the increasing rate and the delay time of the nucleation depended on the Si^+ dose.

The maximum grain was obtained at the dose of 5×10^{15} cm^{-2} and 200 hrs annealing time. The cross sectional TEM was obsearved to investigate the crystallization in the film. Fig.2 shows a growing grain which was on the way to grow. It was known that a grain consisted of a single crystal but there was a large number of dislocations, as shown in Fig.3. It was concluded that the probability of crystal nucleation must be reduced to obtain a film with large grains.

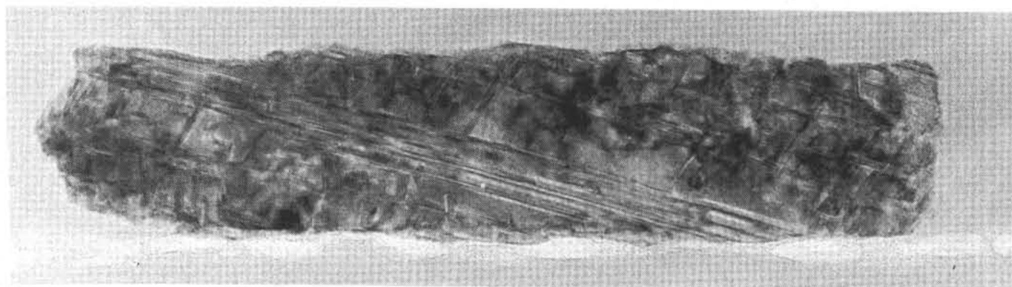
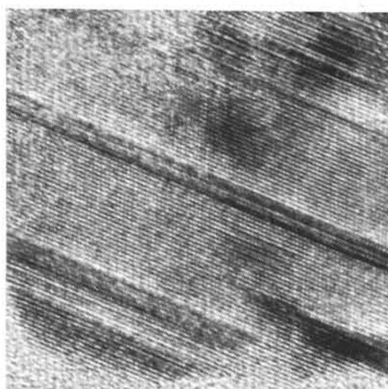


Fig. 2 Cross sectional TEM of a grain

500 Å



50 Å

Fig. 3 Cross sectional TEM in a grain

3. Device fabrication process

Transistors were fabricated in the film prepared by solid phase recrystallization technique. The film was cutted to isolate each transistor. BF_2 ions were implanted at an energy of 70 keV for the control of the threshold voltage. A 500 A thick gate oxide was formed at 1000°C in dry O_2. The polysilicon film was deposited on the oxide and doped with phosphorus. After a photolithography process to form the gate electrode, source and drain region were formed by implantation of As for n-channel and B for p-channel transistors. 1000°C annealing was done to activate the impurity with PSG (Phospho-silicate Glass) as a capping film. Al electrode was used for electrical connection. A plasma-SiN film was used as a passivation film and hydrogenation of a channel polysilicon. The channel length of the transistors studied in the experiment were 2, 4, 6, 8, 10, 12, 16 and 20 μm with the same ratio of the channel width and length. The sheet resistance of the gate, n-channel and p-channel source were 30, 300 and 500 ohm/sq., respectively.

CMOS test elements such as ring oscillator and D-type flip-flop were fabricated on a 5 inch quartz wafer by using the above mentioned process with 7 μm design rule. The photograph of shift resistor is shown in Fig.4.

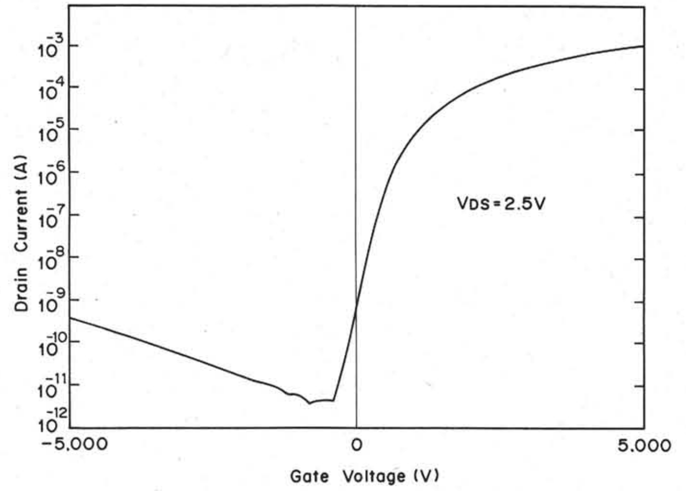


Fig. 5 The characteristics of gate voltage and log (drain current)

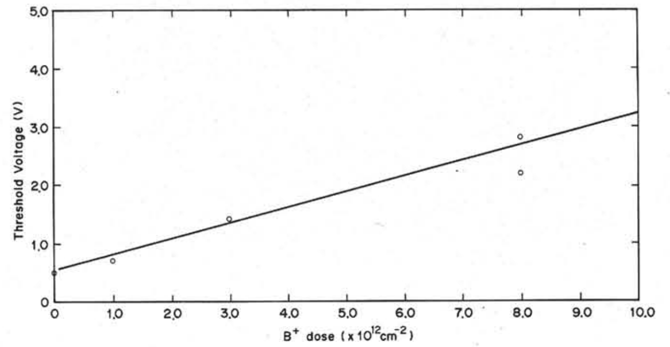


Fig. 6 The dependence of threshold voltage on channel boron dose

4. Results and Discussion

Typical gate voltage vs drain current characteristic is shown in Fig.5, in which W/L of the transistor was 100 μm/10 μm. Vth and field effect mobility of the transistors were plotted against the boron dose in Fig.6 and 7, respectively. It is known that Vth increases linearly with the increase of the channel boron dose, while the mobility decreases with the increase of the channel boron dose of more than 1×10^{12} cm^{-2}, because the electron mobility in the grain was decreased by the ion scattering effect as known in single crystal silicon. Therefore, Vth can be controlled in the range of 0 to 1V without decreasing the mobility in n-channel transistor. Next, the channel length effect was measured. The dependence of the Vth on the channel length is shown in Fig.8. In the channel length less than 2 μm, Vth decreases due to lateral diffusion of impurity from S/D region. The leakage current is plotted against the channel length. A few pA/μm is obtained at 5V except for the short channel of 2 μm.

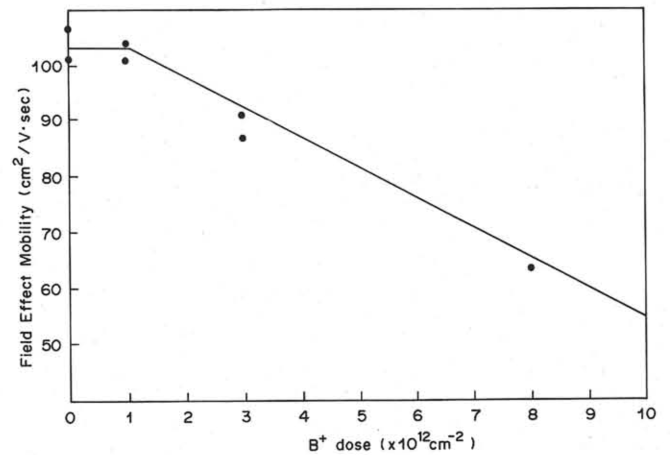


Fig. 7 The relation of field effect mobility and channel boron dose

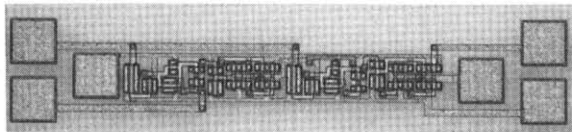


Fig. 4 Microphotograph of CMOS D-type flip-flop

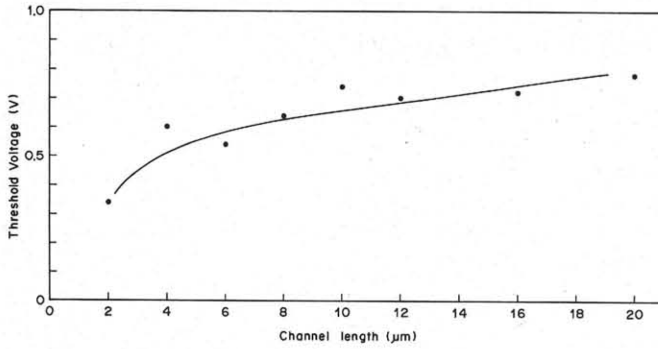
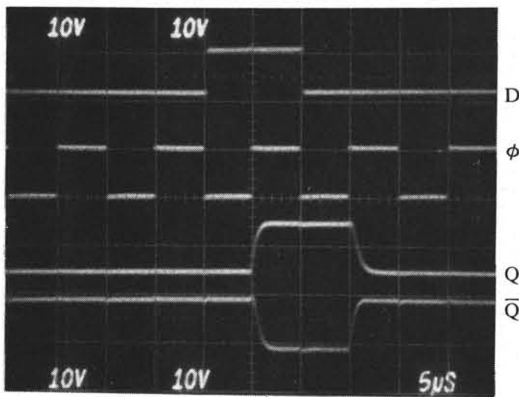


Fig. 8 The dependence of threshold voltage on the channel length



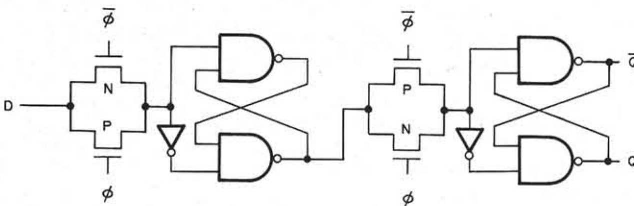


Fig. 9 CMOS D-type flip-flop circuit and operation wave form at 100 kHz

CMOS circuits were studied. Fig.9 shows the circuit of the D-type flip-flop and operation characteristics at 100 kHz. It operated at a maximum frequency of 5 MHz, too. The ring oscillator is operated at the propagation delay time of 3 nsec and the power of 1 mW.

5. Summary

Polysilicon super thin films with large grain size and good quality were developed by using Si^+ implanted amorphization and following solid phase recrystallization. The device on an amorphous insulator was fabricated with a variety of channel length. The process of more than 2 μm design rule can be easily applied to large size monolithic integrated circuits such as linear image sensor, thermal head and ASIC. The typical electrical characteristics were 100 $cm^2/V \cdot sec$ of field effect mobility and pA/μm of leakage current in n-channel transistor. A D-type flip-flop operating at 5 MHz frequency and ring oscillator with 3 nsec delay time were obtained by 7 μm design rule CMOS.

Acknowledgments

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