Electrical and Physical Properties of Rapid-Zone-Recrystallized SOI Made Using a Pulsed Arc Lamp

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Recrystallization using a high-energy pulsed xenon arc lamp line source has produced defect-free single crystal SOI suitable for 3-d IC applications. Material is prepared in a single high-speed scan using whole wafers without the need for a vacuum ambient. Duration of the high temperature cycle is less than 30s. Experiments with seeded samples are described.

Introduction

This paper presents a rapid zone-recrystallization system using a pulsed xenon arc lamp as the zone energy source. The system creates conditions similar to those in line-source e-beam processes without the need for vacuum. The technique can recrystallize an entire three inch wafer in a single pass; therefore this represents a potential high-throughput alternative to raster-scanning spot recrystallization systems for 3-d IC applications.

Simulations of thermal profiles in a rapid zone-recrystallization system[1] indicate that for a given system of films and a zone of fixed power-density, the preheat temperature and scan speed can be optimized to effectively isolate melting in the top SOI layer. Furthermore, variations in the scan speed are seen to be more influential than variations in film thickness, power density, or preheat temperature. Scan speeds must be within 5% of their optimum values (for systems with power densities in the low $kWcm^{-2}$ range) to be applicable to 3-d IC's.

SOI materials preparation techniques include buried insulator[2], and oxidation of porous silicon[3] (both "cold processes"), as well as melt recrystallization using laser[4] or electron-beam spot sources[5] or graphite strip-heater line sources[6]. Of these, only spot recrystallization techniques have been successfully applied to 3-d

IC's for VLSI[7]; common zone-melting systems excessively heat underlying layers, destroying existing structures.

Zone recrystallization produces large area SOI islands and has high throughput. Spot sources are raster-scanned, creating grain boundaries between successive sweeps. To apply zone-melting systems to 3-d IC's, the zone power density must be great enough so that the line width can be narrow while the scan speed is fast enough to prevent overheating existing layers. Line-source e-beams are the only rapid zone-recrystallization systems for 3-d VLSI[8] proposed heretofore.

Experiment

Xenon lamp radiation in high-energy pulses is ideal for efficient energy transfer to preheated Si because it is predominantly in the visible spectrum with less than 1% of the light in the infrared range beyond the absorption cutoff point. Furthermore, low impurity quartz waveguides can be designed to collimate the lamp wall energy; energy transfer efficiencies exceeding 70% are easily obtained without the use of lenses or reflectors.

The recrystallization apparatus is shown schematically in Fig.1. A xenon arc lamp is operated in high-energy pulsed mode. The lamp energy is transferred to the surface of a scanning, preheated three inch wafer via a synthetic quartz plate-optic waveguide. The arc

lamp discharges a multi-stage Guillemin pulse forming network[9], ensuring a constant power density along the zone at the wafer level during the pulse.
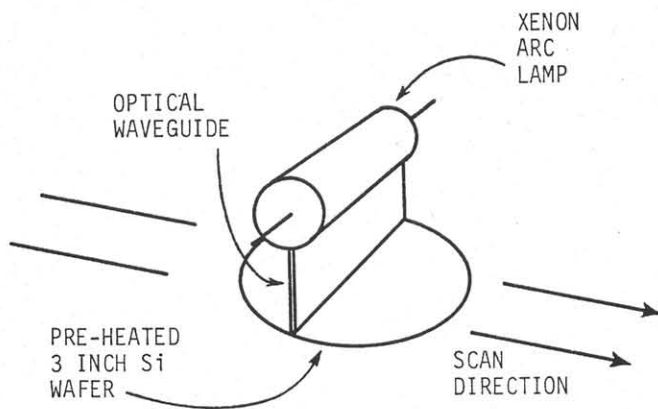

Fig.1: Schematic Representation of Arc Lamp Zone Recrystallization System

Fig. 2 shows a block diagram of the recrystallization system. The patterned wafer is mounted on a translating table and preheated by cw tungsten-halogen lamps to within a few hundred degrees of the Si melting point, to prevent fracture of the wafer due to thermal shock during the pulse. After the sample is appropriately preheated, the translation table accelerates to the desired scan speed and the lamp is pulsed as the wafer passes under the waveguide, thereby zone-melting the surface. The wafer then cools by radiation in a few seconds. The entire duration of the high-temperature process is usually less than 20 seconds, depending on the operating parameters selected.

To assess the various seeding configurations and to determine an optimum combination of film thickness, preheat temperature, and scan speed for obtaining material suitable for active devices, three inch Si wafers were patterned with the seeding test pattern shown in Fig. 3. This pattern has various types of seed windows, such as lines along and against the scan direction, squares and diamond shapes, and chevrons. Scans along the [100] and the [110] direction were both studied. The Si active layer is LPCVD polysilicon on thermally grown SiO_2. Samples were prepared with various insulator thicknesses, as well as several encapsulation configurations.
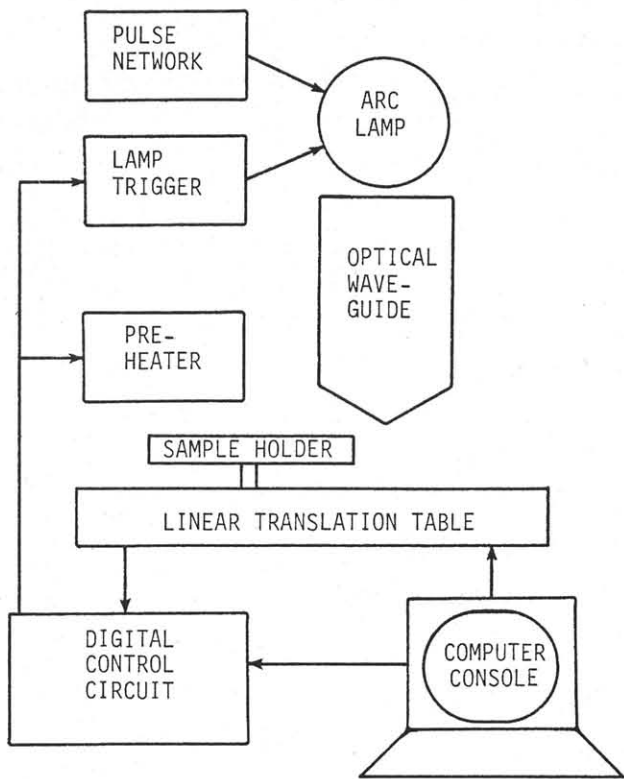

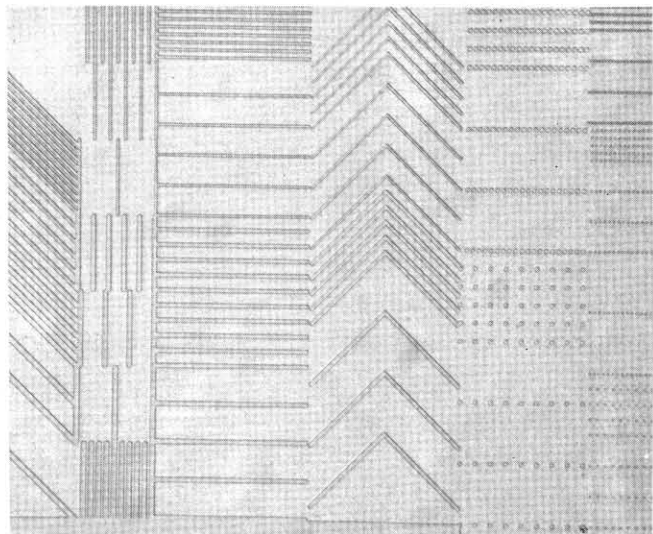**Fig.2:** Recrystallization System Block Diagram

Fig.3: Seed Window Test Patterns for Preliminary Study

The results on the samples made using the mask of Fig.3 indicated a test device mask set should be generated. Electrical measurements on devices processed in recrystallized materials are used to assess the most important SOI materials parameters, namely FET channel mobility, minority carrier lifetime, back-channel leakage, and fixed interface charge density. These parameters are measured using MOSFET's, gate-oxide and insulator

capacitors, junction diodes, PIN diodes, and Schottky barrier diodes; all of these device types are included on the active device test mask.

Experimental Results

Recrystallization of the top Si layer with the substrate orientation was obtained using a wide variety of preheat temperatures, scan speeds, film layer thicknesses, and zone widths. The system power density at the wafer surface was fixed in the 3-4kW cm^{-2} range.

Varying the insulator thickness in the 400 to 1000nm range produced no significant differences, so all ensuing experiments used 500nm oxide insulating layers. The oxide encapsulating layer needs to be 100nm or thicker to prevent agglomeration of the melt, but no significant variation was found in using caps anywhere from 100 to 1000nm thick. Also, no difference was found between deposited or thermally grown capping films. The use of a 50nm Si_3N_4 antireflection film over the cap (50nm being the average quarter-wave value of the chief energy spike in the xenon lamp spectrum) produced a noticeable improvement in energy absorption in the wafers.

The effectiveness of different seed windows varied greatly. Least effective in maintaining the substrate orientation in the top film are the periodically spaced squares or diamonds. Stripes along the zone direction or chevron-patterned windows produce varying results. Smooth SOI of uniform thickness is reproducibly obtained using five or ten micron wide stripes in the direction of the scan, agreeing with results obtained by rapid zone-recrystallization using line-source e-beams[10]. If the seed stripes are spaced over 100 microns apart, the SOI becomes a mixture of seeded material and random spontaneously nucleated islands. Seeded single crystal islands 100 microns wide and up to 2.5 mm long were found. Seeding is appreciably more effective if the scan is along the <100> direction, but scanning along the <110> direction also produces good material.
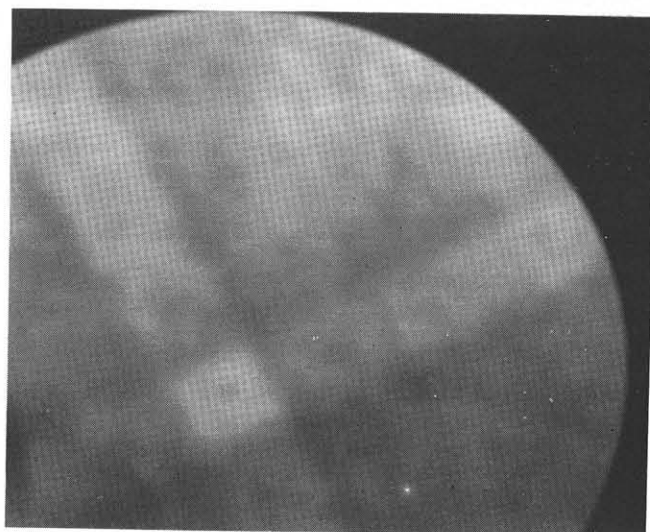
Fig. 4(a) shows an electron micrograph of a recrystallized region of 20 micron wide SOI islands with 10 micron seeds (this region extends the 2.5mm length of the die). The material has been thinned to .25 micron thickness (half the original recrystallized thickness) using Wright
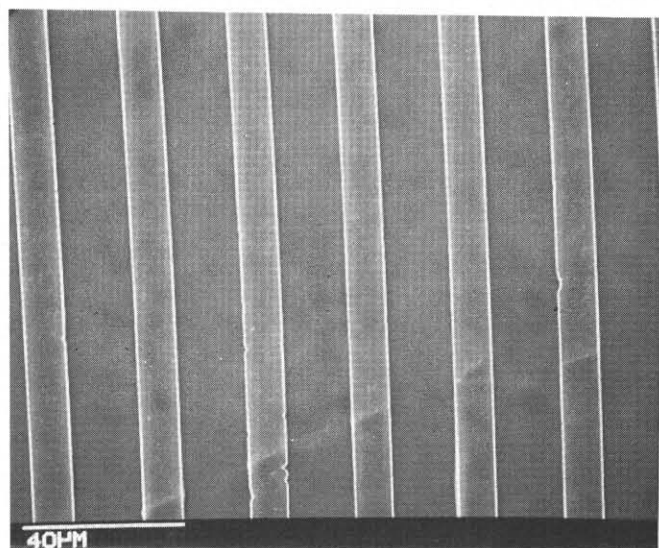
(a)
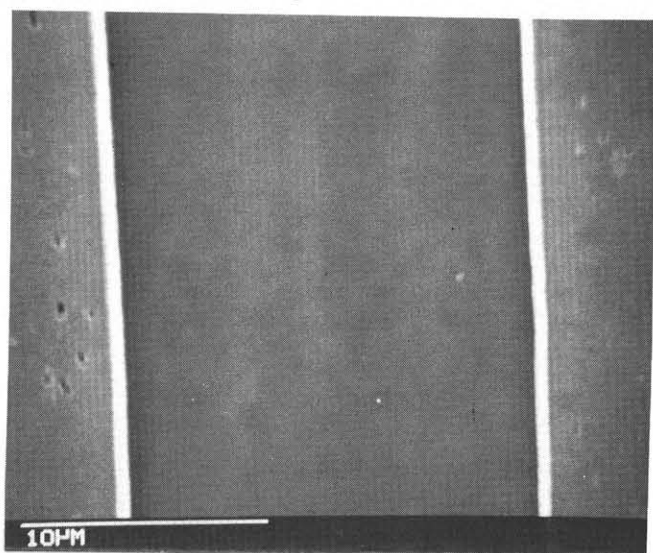
(b)

(c)

Fig.4: **(a)**SEM Micrograph of defect-etched recrystallized region. **(b)**Detail of (a). **(c)**SAD Coates-Kikuchi pattern of detail area.

etch[11] to enhance material defects. Fig. 4(b) shows a magnified view of an area of Fig. 4(a). The material is free of any electrically-active defects. Furthermore, low-angle grain boundaries have not been observed in this material. It is possible that the absence of these defects, commonly seen in slow-scan zone-recrystallized materials, is due to the short time the Si is melted at any specific point which limits oxygen absorption from the surrounding oxides. Fig. 4(c) shows the Selected Angle Diffraction (SAD) pattern of the area in Fig. 4(a). The single bright <100> Coates-Kikuchi pattern verifies that the SOI has the same crystalline orientation as the bulk.

The material in Fig. 4 was preheated to 1375K in 3.5 seconds, scanned at 30 cm/s, and cooled in 8 seconds. As expected from the thermal simulations[12], the preheat temperature could be varied +/- 100C with little change in the resultant material, but the window of suitable scan speeds was about 5%. Obtaining the critical scan speed, where melting is limited to the SOI film, is therefore quite difficult. In samples where the speed deviates from the optimum value, wafer warping can occur. Furthermore, problems with films freezing to non-uniform thickness, layer delamination, and unacceptable surface roughness are noted in samples processed under non-optimum conditions. The recrystallized films are also notably stressed. Occasional shallow ripples at random angles in the top silicon, sometimes extending several hundred micons, have been noted. An example of such a ripple, protruding 10-25 nm, can be seen along the lower area of the material in Figure 4(a).

Summary

A high power density, rapid zone-recrystallization system using a pulsed xenon arc lamp has been developed. SOI material produced from this system has been found to be free of materials defects and suitable for 3-d IC applications. The system has potential for high throughput environments because of its single scan operation on whole wafers without the need for vacuum operation.

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