Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 73-76

Submicron MOSFETs with S/D Diffusions on a Field Insulator

Hiroshi Inokawa, Toshio Kobayashi, and Kazuhide Kiuchi

NTT Electrical Communications Laboratories,
3-1, Morinosato Wakamiya, Atsugi-Shi, Kanagawa Pref., 243-01 Japan

Submicron LID(Lifted Diffused layer) MOSFETs are designed and fabricated to achieve improved speed and power performance. The primary feature of these MOSFETs is that the main portions of the S/D diffusion layers are formed on the field insulator. In addition, structure and processing of the LID-MOSFETs are specially adapted for submicron structures to take full advantage of reduced S/D junction capacitances. Several LID-MOSFETs with gate lengths ranging from 0.5-50 μm and with oxide thickness of 10nm are fabricated, and they all demonstrate good electrical characteristics, such as a maximum transconductance of 118 mS/mm.

1. Introduction

The parasitic capacitance of the source(S)/drain(D) junction comes to limit the speed and power performance of MOSFETs as the device dimensions are reduced to submicron ranges. This is because the lateral dimensions of the S/D junction cannot be scaled proportionally to the dimensions of the active area owing to the necessity of allowing for relatively large alignment error and preventing contact resistance increase.

To reduce the S/D junction capacitance, the unique submicron LID(Lifted Diffused Layer)-MOSFET shown in Fig. 1 has been produced. In this device, major portions of the S/D diffused layers are polycrystalline and are placed on top of the field insulator to reduce S/D capacitance without using SOI[1-3] or a high-resistivity substrate[4]. The channel region is located in a high-quality epitaxial silicon film grown by the well-established CVD technique and is, therefore, directly connected to the substrate to eliminate floating body effects[5].

Structures similar to LID-MOSFET have already been reported[6,7]. However, those structures cannot be used in submicron devices because of the rough surface of S/D polysilicon film deposited under a high-temperature epitaxial condition, and because of the use of the LOCOS technique, which is inadequate for defining the small channel region.

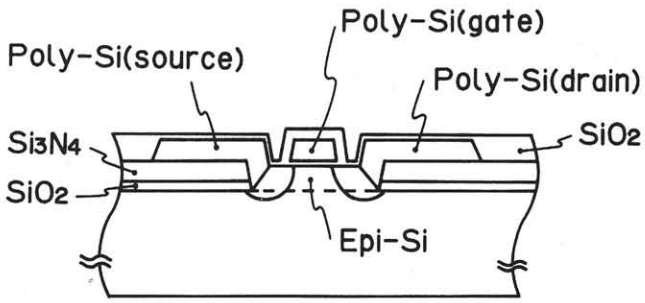

Fig. 1 Cross-section of the LID-MOSFET.

Moreover, the LID-MOSFET has additional advantages as follows. 1) Immunity to the latch-up phenomenon in CMOS circuits is high owing to reduced S/D junction area in contact with the substrate. 2) Junction leakage problems caused by metal penetration or by misaligned contact windows crossing the edge of the S/D region is avoided because the S/D contact area is above the field insulator. 3) The top of gate, source and drain electrodes can exist in a plane because the gate electrode is in a groove.

2. Fabrication technology

LID-MOSFET fabrication steps are as follows. A field insulator consisting of silicon nitride and silicon oxide layers is patterned by an inverted gate mask and anisotropic etching.

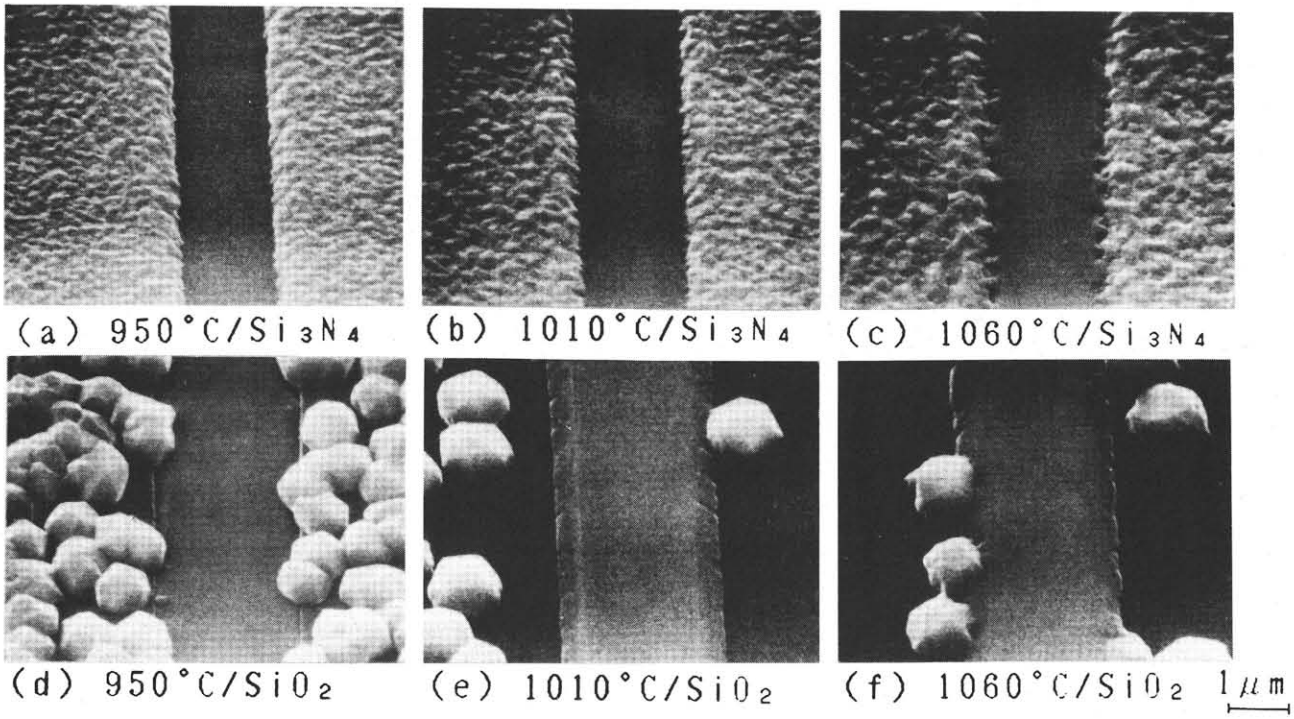

Fig. 2 Surface morphology of polysilicon film on silicon nitride and on silicon oxide, deposited at various temperatures by atmospheric-pressure CVD. Source gas is SiH_4 diluted in H_2 and average film thickness on the silicon nitride is about 400nm. The center of the photograph is an epitaxial silicon film on a silicon substrate.

Then, a 0.19-um undoped silicon film is deposited by atmospheric-pressure CVD at 950°C using SiH_4 as a source gas. An epitaxial layer on the silicon substrate exposed by the etching is used as a channel region, and the polysilicon layer on the field insulator forms the main portion of the S/D diffusion layer. Then the silicon layers corresponding to the source-drain-gate region are isolated by LOCOS. After gate oxidation to 10 nm, boron channel implant and polysilicon film deposition, a polysilicon gate is defined in the groove between the walls of the field insulator using optical lithography and the ECR plasma etching technique[8]. Following fabrication steps of the present LID-MOSFET are the same as those of a conventional n-MOSFET.

To realize a submicron structure, adoption of a field insulator with a nitride top layer, anisotropic etching of the field insulator, and ECR plasma etching of gate polysilicon are essential.

As reported earlier, polysilicon deposited under epitaxial conditions on oxidized silicon tends to have a rough surface owing to the reduced nucleus density[9]. This phenomenon, unsuited for submicron structure, is found to be prevented by using nitride as the top layer of the field insulator. The surface conditions of the polysilicon film deposited on silicon nitride and silicon oxide are compared in Fig. 2. The surface of the polysilicon on nitride (Fig. 2 (a),(b),(c)) is continuous and smooth in contrast to that of polysilicon on oxide (Fig. 2 (d),(e),(f)). The polysilicon on oxide has an island-like morphology and is not continuous. In addition to the use of a nitride layer, silicon deposition temperature is reduced to attain a smoother polysilicon surface. The effect of the reduced deposition temperature is also shown in Fig. 2. Silicon deposition at 950°C on a nitride layer offers a polysilicon surface smooth enough to realize a submicron structure.

Anisotropic etching of the field insulator is necessary for fabricating submicron LID-MOSFETs because high pattern accuracy of the device area is needed to minimize the spacing between the

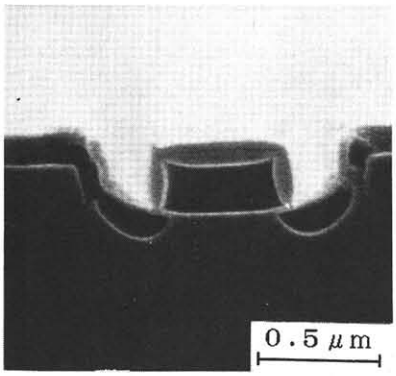

Fig. 3 SEM cross-section of the fabricated LID-MOSFET, slightly etched to delineate gate and S/D diffusions.

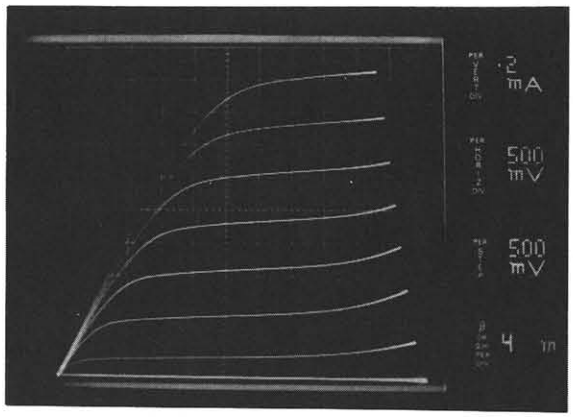

Fig. 4 I_d-V_d characteristics of the LID-MOSFET with gate length of 0.5 μm and gate width of 50 μm.

channel and lifted S/D regions. This reduces the junction area touching the substrate.

ECR plasma etching of the gate polysilicon is also necessary for submicron LID-MOSFETs, in which the gate electrode is placed in a groove. When etching the gate polysilicon in the groove, a high etching rate ratio of polysilicon to silicon dioxide is needed. This is because the thickness in the vertical direction of the polysilicon in the groove is larger than that on the S/D diffused layer by an amount equaling the depth of the groove. In this case, the thin gate oxide (10nm in the present case) must survive during the etching of the polysilicon having a thickness corresponding to the groove's depth (300nm in the present case). In the LID-MOSFET process, anisotropic etching by low-pressure chlorine ECR plasma[8] is used to achieve a selectivity of 60.

A SEM view of the fabricated LID-MOSFET with a 0.5-μm gate length is shown in Fig. 3. It can be seen from the figure that most of the S/D diffusion layer is lifted onto the insulator layer, and the spacing between the channel and lifted S/D regions is very small. ECR plasma etching of gate polysilicon results in a sharply etched profile with no residue.

3. Electrical Characteristics

All of the LID-MOSFETs with gate lengths of 0.5-50 μm exhibit normal FET characteristics. The I_d-V_d and subthreshold characteristics of a LID-MOSFET with a 0.5-μm gate length and a 50-μm gate width are shown in Figs. 4 and 5,

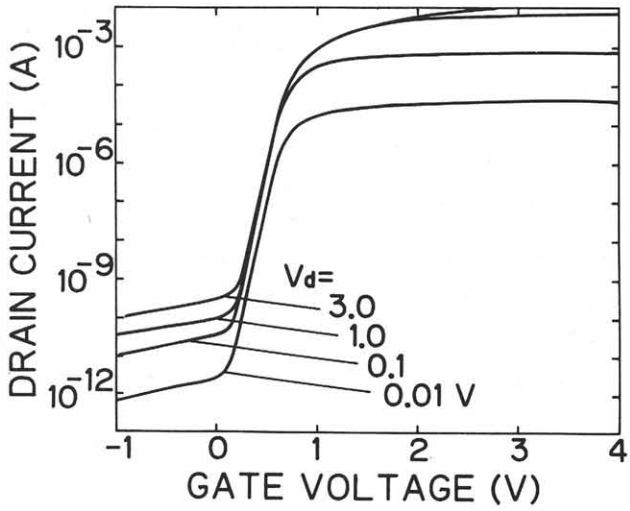

Fig. 5 Subthreshold characteristics of the LID-MOSFET with gate length of 0.5 μm and gate width of 50 μm.

respectively. From the former figure, the I_d-V_d characteristics indicate that the maximum transconductance in the saturation region is 118 mS/mm. From the low-current behavior in the latter figure, it can be seen that subthreshold slope S of the device is 80-82 mV/decade, which is the same as that of the long-channel one. Furthermore, S does not vary with the drain voltage from 0.01 to 3.0 V. This figure also shows that the leakage current per channel length at V_d = 3.0 V and V_g = -1.0 V is about 2 pA/μm.

Using the DC characteristics obtained, inverter delay time in the E/E ring oscillator, whose driver channel width is 10 μm, load channel

overlap capacitance 40 %	gate-channel capacitance 27 %	junction capacitance 33 %

Fig. 6 Relative contribution of capacitances to inverter delay time.

width is 4 μm, and S/D diffusion area of the output node is 54.4 $(\mu m)^2$, is simulated by SPICE. It is found that the inverter delay time is 77 ps/stage in a conventional structure and is reduced by 25% to 58 ps/stage in the present LID-MOSFET structure, because S/D capacitance decreases to one fourth in the latter by placing the S/D diffused layer on a field insulator. The simulation also reveals the relative contribution of S/D junction capacitance, gate-channel capacitance and G-D, G-S overlap capacitance to the inverter delay time. The result shown in Fig. 6 indicates that S/D junction capacitance plays an important role in determining the speed performance of submicron MOS circuits in that the delay time can be reduced to two thirds of its original value by eliminating the junction capacitance.

4. Conclusion

Submicron LID-MOSFETs, whose S/D capacitance is reduced by placing the S/D diffused layer on a field insulator, have been designed and fabricated to attain improved speed and power performance. The main feature of the LID-MOSFET structure is the adoption of a field insulator with a nitride top layer. This nitride layer assists in forming smooth polysilicon S/D regions during high-temperature epitaxial growth of the channel region. The main feature of the fabrication process is the use of highly selective ECR plasma etching of the gate polysilicon in the groove formed between the walls of the anisotropically etched field insulator.

Fabricated LID-MOSFETs with 0.5-50 μm gate lengths and 10-nm oxide thickness have all demonstrated good electrical characteristics. An obtained maximum transconductance of 118 mS/mm along with the reduced S/D capacitance indicates that the present LID-MOSFETs could realize the E/E inverter delay as fast as 58 ps/stage.

References

[1] Y. Kobayashi and A. Fukami, IEEE Electron Device Letters, EDL-5 (1984) pp. 458-460.

[2] B-Y. Tsaur, R.W. Mountain, C.K. Chen, and J.C.C. Fan, IEEE Electron Device Letters, EDL-5 (1984) pp. 461-463.

[3] W. Baerg, J.C. Strum, T.L. Hwa, H.Y. Lin, B.B. Siu, C.H. Ting, J.C. Tzeng, and J.F. Gibbons, IEEE Electron Device Letters, EDL-6 (1985) pp. 668-670.

[4] F.F. Fang and H.S. Rupprecht, IEEE J. Solid-state Circuits, SC-10 (1975) pp. 205-211.

[5] J. Tihanyi and H. Schlotterer, IEEE Trans. Electron Devices, ED-22 (1975) pp. 1017-1023.

[6] J. Sakurai, IEEE J. Solid-state Circuits, SC-13 (1978) pp.468-471.

[7] C.H. Dennison, A.T. Wu, P.K. Ko, C.I. Drowley, and D. Bradbury, Proc. IEDM 85 (1985) pp. 204-207.

[8] T. Ono, C. Takahashi, M. Oda, and S. Matsuo, 1985 Symposium on VLSI Technology (IEEE Cat. No. 85 CH 2125-3) pp. 84-85.

[9] W.A.P. Claassen and J. Bloem, J. Electrochem. Soc., 127 (1980) pp. 194-202.