Electrical Characteristics of Submicron Poly Si MOSFET

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Submicron n-channel Poly Si MOSFETs have been fabricated using thin Poly Si film. The fabrication process includes channel doping, ion-implantation to source/drain region self-aligned to Poly Si gate with side wall spacers and hydrogen passivation. Electrical characteristics are drastically changed and those are strongly dependent on channel doping and gate length. We found that such behaviors were closely related to the activation energy dependence of drain currents on gate bias in the subthreshold region.

§1. Introduction
In recent years, there have been many reports[1],[2] about the applications of fine grain LPCVD Poly Si MOSFETs to Si LSI. Poly Si MOSFETs can be integrated and scaled down just in the same manner as 2-dimensional Si LSI by conventional fabrication processes in spite of its inferior characteristics in comparison with recrystallized Si transistors which are very popular as SOI transistors. If the application areas of Poly Si MOSFET are well selected, we could achieve high density 3-dimensional LSI with specific characteristics.

The benefit of hydrogen passivation [3],[4] and thin Poly Si[5] have been already proposed. We have combined these attractive processes and fabricated submicron Poly Si MOSFET. This paper reports the fabrication process of Poly Si MOSFET and gate length and channel doping dependence of n-channel Poly Si MOSFETs characteristics.

§2. Fabrication
The fabrication process of n-channel Poly Si MOSFET is schematically shown in Fig.1. Experimental test devices were fabricated onto a 500nm of thermally grown oxide. A 110nm thick Poly Si was deposited at 620°C by a conventional LPCVD system. Device isolation was accomplished by RIE. Poly Si islands were oxidized at 1000°C in dry oxygen for 100min. Poly Si oxide thickness was 65nm and Poly Si thickness was about 70nm after oxidation. Arsenic or boron was implanted to various doses to adjust the channel doping. A 450nm thick Poly Si was deposited by LPCVD, doped by POCl3 diffusion at 900°C, and etched by RIE, to form gate electrode. Side-wall spacers were formed by a 0.4μm thick CVD SiO2 deposition followed by RIE. Arsenic with a dose of 3E15cm-2 was implanted to source/drain region self-aligned to n-PolySi gate with the side-wall spacers as a mask. Following a 600nm thick PSG deposition, devices were annealed at 950°C in N2 for 20min. After opening contact holes, a 1.1μm thick Al-Si was deposited and then patterned. Devices were finally hydrogen-passivated after sintering at 440°C in H2. Hydrogen passivation was performed in hydrogen and nitrogen plasma at 300°C, 1torr for 2hours. All of lithography and etching steps were performed by stepper and RIE, respectively.

There are 4 key process steps in our fabrication.
(1) using thin Poly Si
Since Poly Si thickness after oxidation becomes much thinner than the maximum depletion layer width and the channel is fully depleted, threshold voltage and leakage current can be markedly improved. High temperature oxidation
causes the enhancement of Poly Si grain growth[5]. We found that average grain size of Poly Si, whose thickness as grown was 100nm, increases to about 60nm after oxidation at 1000°C in dry oxygen for 100min, but afterwards further grain growth does not occur.

(2) channel doping

The grain boundary property, which plays an important role in the electrical conduction in Poly Si, might be changed by impurities. We could control the characteristics of Poly Si MOSFET to be suitable for specific applications by optimizing channel doping. As will be mentioned later, the characteristics are drastically improved by channel doping.

(3) implantation to source/drain self-aligned to n-Poly Si gate with side-wall spacers

Since the lateral diffusion into the channel region is suppressed, effective channel length gains the width of side-wall spacers. Side-wall spacer has advantage to short channel devices.

(4) hydrogen passivation

Hydrogen atoms introduced into devices in hydrogen plasma passivate the localized states at the grain boundaries and Si-SiO2 interface. They improve field effect mobility and threshold voltage, and the decrease of leakage current.

We could achieve 0.8μm gate length Poly Si MOSFET by these key processes.

§3. The characteristics of Poly Si MOSFETs

A photograph of Poly Si MOSFET is shown in Fig.2. The gate length and width are 0.8μm and 25μm, respectively.

Fig.3 shows Id-Vg characteristics of Poly Si MOSFET with several gate lengths for three different channel doping at Vd=5V. It shows that leakage current is invariant with channel length, but dependent on channel doping. Boron doped Poly Si MOSFETs have sufficiently small leakage current. Leakage current is assumed to originate via field emission through grain boundary traps at drain junction[6].

Fig.4 shows threshold voltage as a function of gate length. Threshold voltage is obtained from the linear region Id/Vg characteristics. In the devices with channel length longer than 5μm, threshold voltage is almost invariant with channel doping. For Arsenic doped and undoped Poly Si MOSFETs, we found short channel effect, which is a threshold voltage lowering. On the other hand, with Boron doped version, we did not find such an effect.

Fig.5 shows gate length dependence of drive currents which is drain current at Vg=Vd=5V. Drive currents for undoped and As doped Poly Si MOSFETs exponentially increase but that drive currents for Boron doped versions increase slightly with decreasing gate length. The increase of drive currents in the shorter channel devices than 5μm might be mainly caused by threshold voltage lowering with decreasing gate length. But for the longer devices, since threshold voltage is almost invariant with channel doping as mentioned above, it can not be explained only by threshold voltage. Drain current is dominated by potential barrier at grain boundaries and junction, which are modulated by gate bias[7].

Fig.6 shows inverse subthreshold slope of Poly Si MOSFETs as a function of gate length in comparison with bulk Si and laser recrystallized Si transistors. Inverse subthreshold slope is a suitable parameter to consider the influence of grain boundary properties in the subthreshold region. For Arsenic doped and undoped Poly Si MOSFETs, it drastically improves with decreasing gate length. On the other hand, for lightly Boron doped version it slightly improves, but with Boron dose larger than 2E13cm-2 it degrades. For bulk Si and laser recrystallized Si transistor, significant change is not found except for increase in short channel laser recrystallized Si ones.

Fig.7 shows activation energy of drain current as a function of gate bias. It is profound through the temperature dependence of drain current in the temperature range between room temperature and 150°C at Vd=50mV. Activation energy relates closely to the potential barrier at the grain boundary[7] and is modulated by gate bias[8], unlike in resistors. We define the efficiency of gate bias modulation as the maximum value of dEa/dVg in the subthreshold region. dEa/dVg is shown as a function of gate bias in Fig.8. In the undoped Poly Si MOSFET,
dEa/dVg rapidly increases with decreasing gate length. It is assumed that in short channel devices, arsenic atoms introduced by lateral diffusion from source/drain into channel region strongly influence the potential barrier at the grain boundary, hence the conduction. On the other hand, for the doped versions, dEa/dVg is invariant with channel length. In these cases, channel doping determines the conduction in the channel. For Arsenic dose at $1E12cm^{-2}$, potential barrier at the n+n Junction is small, dEa/dVg is reduced. For Boron doped devices, dEa/dVg is nearly constant with channel length, but drastically changes through Boron doping. dEa/dVg of Poly Si MOSFET with Boron dose at $5E12cm^{-2}$ is very large and potential barrier at the grain boundary is well modulated in that MOSFET. But above $2E13cm^{-2}$, dEa/dVg becomes small and gate bias modulation degrades. These behavior of dEa/dVg is in good agreement with that of inverse subthreshold slope.

§4. Conclusion

We have achieved submicron Poly Si MOSFETs by using 4 beneficial process steps. The characteristics of Poly Si MOSFETs are improved with decreasing gate length. Gate length dependence of the characteristics drastically changes by channel doping. Lightly Boron doped Poly Si MOSFET, whose Boron dose is about $5E12cm^{-2}$, has small leakage and good subthreshold characteristics, which are almost independent of gate length. Subthreshold characteristics are closely related to the maximum of dEa/dVg, which is assumed to correspond to the modulation of potential barrier at grain boundaries by gate bias.

Reference

Nch. Poly Si MOSFETs

Fig. 3 Id-Vg characteristics of Poly Si MOSFETs with several gate lengths for three different channel dopings at V_d=5V. Gate length of (a), (b), (c), (d) and (e) are 0.8, 1.0, 1.4, 3.4 and 4.4μm, respectively. Gate width is 25μm. Drain bias is 5V. CD means channel dose.

Fig. 4 Threshold voltage (V_th) as a function of gate length (L).

Fig. 5 Drive current as a function of gate length (L) at V_g=V_d=5V.

Fig. 6 Inverse subthreshold slope (S) as a function of gate length (L) in comparison with bulk Si and laser recrystallized Si transistors.

Fig. 7 Activation energy (E_a) of drain current as a function of gate bias (V_g). Circle, triangle and square denote the activation energy of Poly Si MOSFETs whose gate length are 4.4, 1.0 and 0.8μm, respectively. Gate width is 100μm.

Fig. 8 The efficiency of gate bias modulation (dE_a/dV_g) as a function of gate length (L).