Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 85-88

PARAMOST - A New Parasitic Resistance Model for Deep Submicron MOS Transistors

Kazuo Yano, Masaaki Aoki, and Toshiaki Masuhara

Central Research Laboratory, Hitachi Ltd.

Kokubunji, Tokyo 185, Japan

A new parasitic series resistance model for submicron MOSFET is proposed and experimentally verified. The model precisely takes into account the existance of parasitic resistance and thus can accurately predict major MOSFET parameters such as drain current, threshold voltage, subthreshold swing and breakdown voltage. This is the first time that the back bias effect due to parasitic resistance is introduced in the model. The model is used to estimate the performance of a 100nm CMOS device. The model suggests, that in the sub-300nm region, the decrease in the drain series resistance is of special importance to decrease the switching delay.

1. INTRODUCTION

Parasitic resistance due to source and drain diffusion layers, current crowding, [1] and metal-silicon contact is one of the major constraints on the high-speed operation of submicron CMOSs[2]. Therefore, the optimum design of drain structures and the precise estimation of their performance and reliability are becoming one of the major concerns in VLSI device engineering. Recently, several models including parasitic resistance [3][4] have been proposed for the estimation of the MOSFET parameters. However, these models do not accurately take into account the modulation of parameters due to parasitic resistance.

In this paper, a new parasitic resistance model called PARAMOST (parasitic resistance analysis in MOS transistors) is proposed. Using PARAMOST, precise evaluation of major MOSFET parameters as influenced by parasitic resistance is possible. The basic formulation, experimental verification, and application to the performance estimation of 100nm CMOS device are given. Special emphasis is placed on estimating the performances of CMOS device operating at 77K[5][6].

2. PARASITIC RESISTANCE MODELLING

Previous models[3][4] assumed that the effect of source and drain parasitic resistance was represented by an IR drop in only drain and gate biases as shown by:

$$V_{Gi}=V_G-I_DR_S \quad (1)$$

$$V_{Di}=V_D-I_D(R_S+R_D), \quad (2)$$

where subscript i denotes an intrinsic MOS transistor in which parasitic resistance is excluded. However, the doping density of the substrate increases as the device dimensions shrink, according to the scaling rule[7]. In the present model, back bias due to the parasitic source resistance shown in Fig.1 is taken into account as follows:

$$V_{Bi}=V_B-I_DR_S \quad (3)$$

Employing Eqs.(1), (2), and (3), the drain current is expanded into series with respect to R_S and R_D as:

$$I_D=I_{Di}-g_{mi}I_DR_S-g_{Di}I_D(R_S+R_D) -g_{Bi}I_DR_S+o(R_S)+o(R_D), \quad (4)$$

where g_B is the substrate transconductance. Neglecting the higher order terms, the drain current is approximated by:

$$I_D=I_{Di}/(1+g_{mi}R_S+g_{Di}(R_S+R_D)+g_{Bi}R_S). \quad (5)$$

In Eq.(5), $g_{mi}R_S$, $g_{Di}(R_S+R_D)$, and $g_{Bi}R_S$ express the negative feedback on the gate, drain, and substrate voltages, respectively. When R_S equals R_D, Eq.(5) is simplified to Eq.(6) in Table 1.

Using Eq.(6), Equations (7)-(10) summarized in Table 1 are derived. Analytical Eqs.(6)-(10) represent the PARAMOST model. Major MOSFET parameters as influenced by arbitrary parasitic

resistance are estimated using PARAMOST as shown next.

3. EXPERIMENTAL VERIFICATION AND ANALYSIS

The MOSFETs measured are fabricated using double well CMOS technology and have a gate oxide thickness of 25nm and n^+p and p^+n junction depths of 0.25μm and 0.4μm, respectively. N-channel MOSFETs with a conventional single drain (SD) and a lightly doped drain (LDD) are fabricated. In addition, p-channel MOSFETs with a conventional single drain are made. The n^-region in the LDD is formed by phosphorous implantation with a junction depth of 0.2μm, and an n^- dose of $1x10^{13}cm^{-2}$ at 50KeV.

PARAMOST, Eqs.(6)-(10), is experimentally verified by connecting the external resistances in series. For calculations, parameters I_D, g_m, g_D, and g_B, which are measured under specific bias conditions, are employed. The measured dependence of the drain current on external resistance is shown in Fig.2. The agreement between the values calculated by Eq.(6) and the measured ones is excellent at room and liquid nitrogen temperatures and in linear and saturation regions.

The dependence of measured g_m on external resistance is shown in Fig.3. The agreement between calculated and measured values is again excellent. Usually, a formula[8] is employed to calculate the dependence:

$$g_m=g_{mi}/(1+g_{mi}R_S). \tag{11}$$

The formula, however, is inaccurate as shown in Fig.3 because it neglects the negative feedback effect on drain and substrate voltages. This can be easily proven by estimating the contribution from g_m, $2g_D$, and g_B as follows. In the saturation region, the relative measured conductance of a 0.64μm MOSFET's g_m, $2g_D$, and g_B are 1, 0.37, and 0.12 at 300K and 1, 0.46, and 0.13 at 77K, respectively. Neglecting g_D and g_B causes an underestimation of the parasitic resistance effect that can equal over thirty percent.

PARAMOST can also be applied to evaluate the drain breakdown voltage as affected by the parasitic resistance. The dependence of measured drain breakdown voltage on parasitic resistance is shown in Fig.4. The agreement between calculated and measured values is again excellent for SD and LDD structures. It can be seen that the breakdown voltage in the LDD is higher than that in the SD, even when the transistors have the same parasitic resistance. This difference is caused by a field reduction due to the LDD having a more highly graded junction. In other words, the breakdown voltage enhancement in the LDD of 3.1V over SD arises from two factors: an IR drop of 0.4V due to resistance and a field reduction of 2.7V. The main origin of this LDD breakdown voltage enhancement is concluded to be the field reduction due to the graded drain junction. This is the first time these field reduction and IR drop factors have been identified.

Next, a new procedure for evaluating the intrinsic MOSFET parameters using PARAMOST model is provided. To calculate the intrinsic drain current I_{Di} and transconductance g_{mi} from actual values, following expressions can be easily obtained by using Eqs.(6) and (7):

$$I_{Di}=I_D/(1-gR_S) \tag{12}$$

and

$$g_{mi}^{sat}=g_m^{sat}/(1-gR_S) +I_{Di}R_S(\partial g_i/\partial V_{Gi})/(1-g_iR_S)^2. \tag{13}$$

To obtain both I_{Di} and g_{mi}, I_D, g_m, g_D, and g_B are measured at various channel lengths for single drain devices. R_S is also measured by Chern's method[9] for single drain devices. By using the values in Eq.(12), the drain current for intrinsic MOSFETs free from the influence of the parasitic resistance effect can be calculated. The results are shown in Figs.5 and 6. In the figures, an evident saturation of drain current is observed in short channel MOSFETs, even if the parasitic resistance effect is excluded. This result suggests that the velocity saturation effect is the major cause for the measured saturation of drain current in submicron MOSFETs. This is the first time that the precise exclusion of series resistance from measured drain current has been reported.

In Fig.5, significant LDD drain current reduction at 77K is observed, especially in the linear region. This reduction is caused by carrier freeze-out in the n^- offset region. Therefore, optimum design of the n^- region, which minimizes the carrier freeze-out effect, is

required for high-speed operation of LDD MOSFETs at 77K.

4. PERFORMANCE ESTIMATION OF 100nm CMOS

PARAMOST is utilized to estimate the inverter delay of submicron CMOSs as shown in Fig.7. The inverter delay is estimated to be the product of inverse saturation current, supply voltage, and load capacitance. Considering the limitations due to hot carrier degradation, constant field scaling[7] is assumed, except in the case of threshold voltage, which is assumed to be constant. Threshold voltages are assumed to be 0.5V and 0.2V at 300K and 77K, respectively. In Fig.7, the minimum delay time is observed with decreasing gate length. The reason is that the non-scalable threshold voltage significantly reduces the effective gate voltage swing as the supply voltage is reduced. The gate length giving the minimum is smaller at 77K than at 300K. This is because the subthreshold swing is smaller at 77K than at 300K by a factor of kT/q. This is the most obvious advantage of low temperature operation of CMOSs.

A significant increase in delay due to parasitic resistance is observed in short channel CMOSs. The increase is by a factor of 2 at 300K and by a factor of 4 at 77K when the resistance is 1.5ohm.mm, which is typical of the LDD structure. Thus, source and drain parasitic resistance is the most significant constraint on performance improvements in deep submicron CMOSs and ,especially, in devices operated at 77K.

5. CONCLUSION

A set of simple analytical equations that takes the parasitic resistance effect into account is proposed. It is called PARAMOST. The negative feedback due to drain conductance and substrate transconductance is found to cause significant reduction in drain current in the submicron region. The usefulness of PARAMOST is demonstrated by calculating the drain current and breakdown voltage tradeoff, intrinsic drain current, and 100 nm CMOS performance. In a sub-300nm CMOS device the decrease in parasitic series resistance is of special importance for decreasing the switching delay.

ACKNOWLEDGEMENT

The authors wish to thank Dr.Shojiro Asai and Messrs.Yoshio Sakai, Tohru Kaga, Osamu Minato, and Masakazu Aoki of Hitachi Central Research Laboratory for valuable discussions. In addition, they also would like to express their appreciation to Messrs.Satoshi Meguro and Shuji Ikeda of Hitachi Musashi Works for sample fabrication.

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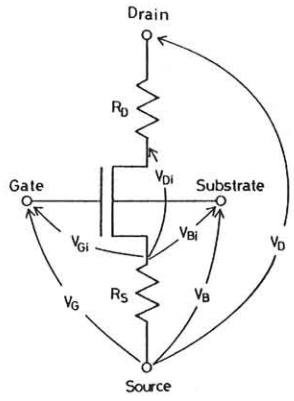

Fig.1 Equivalent circuit of MOSFET with parasitic resistance.

Table 1 Formulas for PARAMOST Model

Drain Current	I_D	$I_D = \frac{I_{Di}}{1 + g_i R_s}$	(6)
Transconductance	g_m	$g_m = \frac{g_{mi}}{1 + g_i R_s} - \frac{I_{Di} R_s}{(1+g_i R_s)^2} \frac{\partial g_i}{\partial V_{Gi}}$	(7)
Breakdown Voltage	BV	$BV = BV_i + (\frac{g_{Bi}}{g_{Di}} + \frac{2}{1 + g_i R_s}) I_{Di} R_s$	(8)
Threshold Voltage	V_T	$V_T = V_{Ti} + I_{Di} R_s g_i / g_{mi}$	(9)
Subthreshold Swing	α	$1/\alpha = 1/\alpha_i - \frac{R_s}{1+g_i R_s} \cdot \frac{\partial g_i}{\partial V_{Gi}}$	(10)

$g_m = \partial I_D / \partial V_G$, $g_D = \partial I_D / \partial V_D$, $g_B = \partial I_D / \partial V_B$, and $g = g_m + 2g_D + g_B$

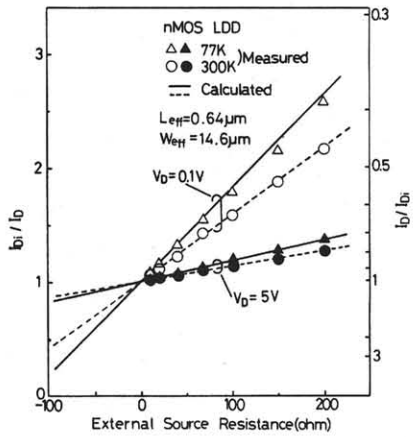

Fig.2 Dependence of drain current on external resistance. R_D is assumed to be equal to R_S.

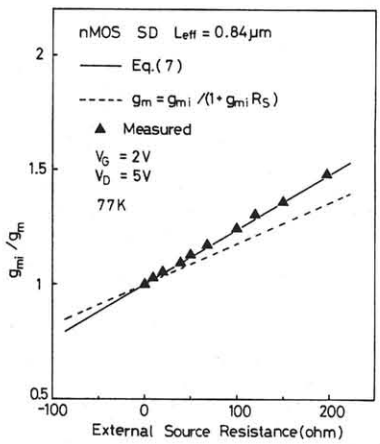

Fig.3 Dependence of transconductance on external resistance. R_D is assumed to be equal to R_S.

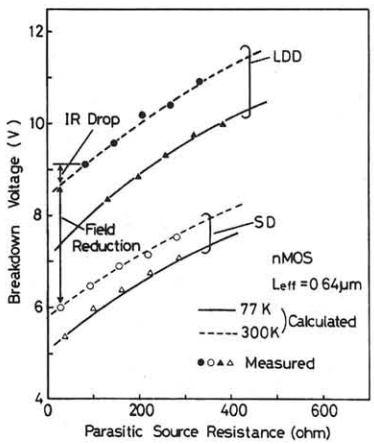

Fig.4 Dependence of drain breakdown voltage on parasitic resistance. R_D is assumed to be equal to R_S.

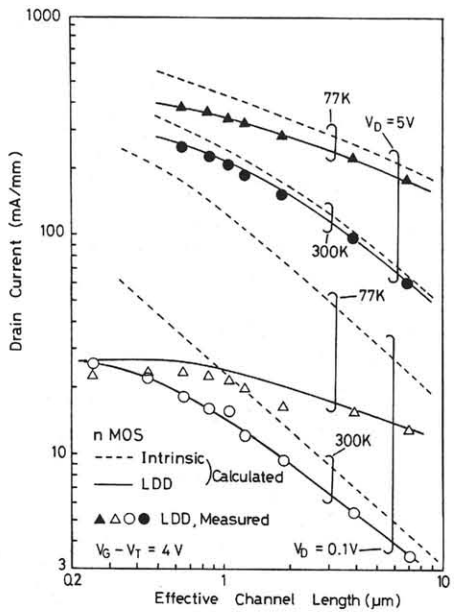

Fig.5 Drain current of intrinsic and LDD n-channel MOSFET vs. effective channel length.

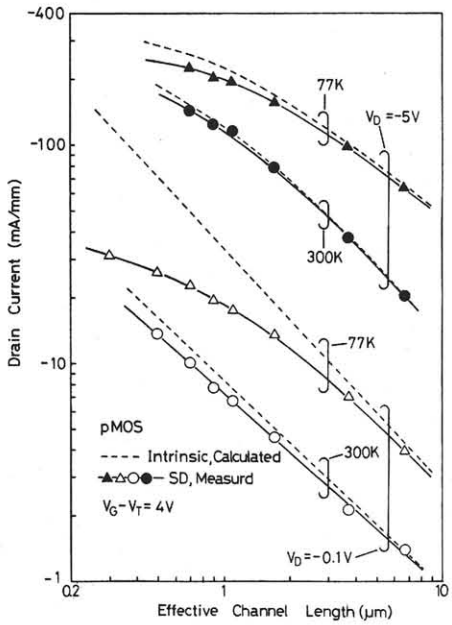

Fig.6 Drain current of intrinsic and SD p-channel MOSFET vs. effective channel length.

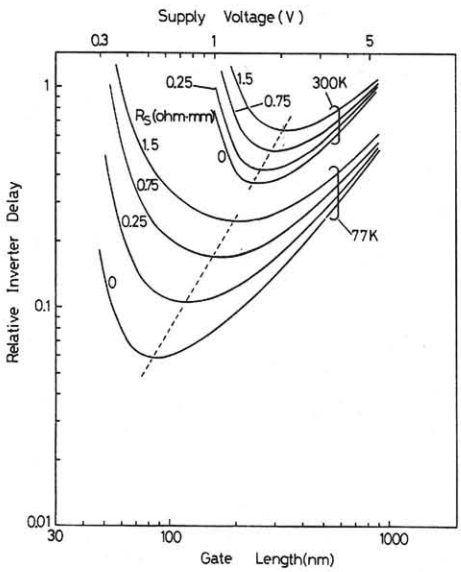

Fig.7 Calculated dependence of inverter delay on gate length.