Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 89-92

1800V Non-Latch-Up Bipolar-Mode MOSFETs(IGBT) Fabricated by Silicon Wafer Direct Bonding

Akio Nakagawa, Yoshihiro Yamaguchi, Kiminori Watanabe
Hiromichi Ohashi, Masaru Shimbo

Toshiba Research & Development Center

1 Komukai Toshibacho, Saiwai-ku, Kawasaki, 210
Japan

1800V 10A Bipolar-Mode MOSFETs have been developed, based on Silicon Wafer Direct Bonding (SDB) technique: a new substrate wafer fabrication process superior to conventional epitaxy. The SDB technique easily realizes an optimum N buffer structure as well as a high resistivity N^- layer. An amorphous silicon resistive field plate has been implemented for 1800V breakdown voltage. 0.45μsec. fall-time and 150A maximum current capability have been successfully realized.

1. Introduction

It has become widely recognized that a Bipolar-Mode MOSFET [1] is a nearly ideal power device, especially for a high voltage range (≳300 V) owing to its high switching speed [2,3], large current capability [3,4] and large SOA [5]. For example, the chip area for a 1000 V Bipolar-Mode MOSFET is less than a twentieth of the chip area for an equivalent conventional power MOSFET. Latch-up of the parasitic thyristor, which is the only shortcoming for the composite device, has been successfully suppressed so that the current capability for Bipolar-Mode MOSFETs is larger than that for bipolar transistors and for conventional power MOSFETs. More than 20 KHz high frequency operation can easily be attained by the Bipolar-Mode MOSFETs, realizing low noise inverter systems.

This paper present 1800 V Bipolar-Mode MOSFETs for the first time anywhere in the world. Two major breakthrough technologies were developed for 1800 V devices. One is silicon wafer direct bonding (SDB) technique: a new silicon wafer fabrication process superior to conventional epitaxy. A high resistivity layer as well as an optimum n-buffer structure were easily realized by the SDB technique. The other was a new junction termination technique: a combination of metal field plate and amorphous silicon resistive field plate [6]. The adequately combined two structures attained 1800 V breakdown voltage for a junction termination area as narrow as 450 μm.

The developed 1800 V 10 A Bipolar-Mode MOSFET exhibits excellent electrical characteristics: 4.5 V forward voltage drop for 10 A (50 A/cm^2) drain current, 0.45 μsec fall time and more than 150 A current capability. Latch-up current density is sufficiently large so that allowable power dissipation exceeds the theoretical limit (3×10^5 watt/cm^2) for bipolar transistors. Moreover, safe operating area (SOA) is greater than the saturation current for 15 V gate voltage and 1000 V drain voltage. Owing to these characteristics, Bipolar-Mode MOSFETs can be used in the same way as ordinary bipolar transistors without paying any attention to latch-up. This is why this device is called a "non-latch-up Bipolar-Mode MOSFET".

2. Silicon wafer direct bonding (SDB) technique

It has long been a dream for device engineers to realize any desired impurity profiles by bonding a number of sliced silicon wafers with various thicknesses and resistivities. Now, it is no longer a dream, although its applications are currently limited. We developed this technology to realize an optimum n-buffer structure as well as a high resistivity layer on the n-buffer layer.

Silicon wafer bonding was carried out by facing and pressing two mirror polished wafer surfaces after hydrophilizing surface treatment. Bonding as rigid as the original bulk material is achieved by thermal treatment at more than 1100°C ambient temperature [7].

The SDB process sequence applied to the 1800 V devices is shown in Fig. 1. First, a mirror polished high resistivity bulk wafer and a low resistivity P^+ substrate wafer were prepared. An n type dopant such as phosphorus was implanted into the mirror surface of the high resistivity bulk wafer and was driven-in to form an n^+ diffusion layer. Then, a p type dopant such as boron was introduced, forming a shallow p diffusion layer on the n^+ layer. Finally, the two mirror surfaces of the p^+ substrate and the bulk wafer were bonded in the manner stated above to form an $n^-/n^+/p^+$structure. The thickness of the high resistivity n^- layer can be adjusted by conventional lapping technique. Figure 2 shows the measured spreading resistance profile for the fabricated $n^-/n^+/p^+$ structure. Neither discontinuity nor electrical barrier were observed at the bonded interface. Ordinary MOSFET fabrication processes are applied to the thus bonded wafers, yielding Bipolar-Mode MOSFETs. Because a large number of lattice defects exist at the bonded interface at present, SDB should not be done inside the device, where large carrier lifetime is required.

3. A new junction termination technique

High withstanding voltage has to be realized with the use of shallow diffusion layers because shallow junctions are generally used in power MOSFETs for low on-resistances. A good junction termination method should attain a nearly ideal breakdown voltage with shallow junctions without consuming large peripheral chip area. It was found that an optimized combination of a resistive field plate and a metal field plate easily realize 1800 V breakdown voltage (80% of ideal breakdown voltage) with an only 450 μm wide junction termination area and 10 μm deep diffusion layers. Figure 3 shows the structure adopted for 1800 V devices. A source metal layer extending over a thick oxide film serves as a metal field plate. A high resistance a-Si film deposited over an oxide film and metal layers create a linear potential gradient on the thick oxide film. The combined structure smoothly terminates the depletion layer created by the applied voltage. Withstanding voltage has its maximum for an optimized metal field plate length. This phenomena can be clearly shown in Fig. 4 by a numerical simulation [6].

4. Electrical characteristics and Safe Operating Area

The design theory for 1800 V Bipolar-Mode MOSFETs was basically the same as those for 1200 V and 600 V devices. Stripe source gate pattern [8], n-buffer layer [1], double p-base diffusion [1] were still adopted for non-latch-up characteristics and low forward voltage. Latch-up current density for the turn-off transient is more than 150 A (at 25°C), which is far larger than the rated current 10 A so that the devices can be regarded as non-latch-up devices if the gate voltage is kept not greater than 15 V.

Figure 5 shows an overview of a fabricated 1800 V 10 A device. The chip size is 6x6 mm^2 and the active region is 20 mm^2. The obtained trade-off curve for a 1800 V device is shown in Fig. 6 (see curve A). A short fall time 0.45 μsec is attained for 4.5 V forward voltage drop.

SDB technique easily attains an optimum n-buffer condition. Excessively high n-buffer impurity concentration deteriorates device forward voltage, whereas low n-buffer concentration does not improve the trade-off relation between forward voltage drop and fall time. It is extremely difficult to epitaxially grow a high resistivity and thick n-layer on a high impurity concentration substrate. Compromizes had to be accepted for the n-buffer/p^+ substrate impurity concentration so that high resistivity n-layer could be grown on the substrate wafer. An optimum n-buffer condition can only be realized by the SDB technique, exhibiting a best trade-off (curve B in Fig. 6) as well as a higher breakdown voltage 1400 V, compared with epi-wafer devices (see curve C, D in Fig. 6). Trade-off curve C, which is the best one among those for the devices fabricated on epi-wafers, was attributed to a device fabricated on epi-wafer 1, which closely reproduced an optimum n-buffer condition. However, this epi-wafer 1 could not be mass-produced because of difficulties.

Figure 7 shows high voltage high current saturation characteristics obtained by 10 μsec DC pulses. Power dissipation exceeded $8x10^5$ W/cm^2, which is far larger than the critical value ($2 \sim 3x10^5$ W/cm^2), which is assumed to be the theoretical avalanche limit for bipolar transistors. As Bipolar-Mode MOSFETs operate in double injection mode, this limit value does not apply to the present case. (However, this limit has a meaning for the turn-off transient after electron channel current ceases.) It is manifest from Fig. 7 that latch-up does not occur up to 160 A drain current. (Latch-up phenomena can be observed within 10 μsec and usually it destroys the tested device.)

Typical 100 A switching-off waveforms are seen in Fig. 8. The observed fall-time is 300 nsec., which is shorter than that for a small current case.

Safe operating area for 1800 V Bipolar-Mode MOSFETs was measured by the same circuit (see Fig. 9) as was used for 1200 V devices. The test device was directly connected to a constant voltage source, whose voltage was varied from 800 V to 1100 V. The device was switched-on for 10 μsec and then switched-off. The drain current was increased by raising the on-gate voltage. The drain voltage was kept the same as constant voltage source voltage V_A except for switching transients. The broken line in Fig. 7 shows maximum drain current I_{DM} just before the turn-off vs. on-state drain voltage (= constant voltage source voltage V_A) characteristic. As maximum drain current I_{DM} is limited by the failure at the turn-off transients, the broken line in Fig. 7 shows SOA for switching transients after 10 μsec $I_{DM} \cdot V_A$ watt power dissipation. Figure 10 shows typical waveform for this test. This type of SOA is called "short-circuited SOA" in this paper. "Forward SOA without gate turn-off" is assumed to be greater than this short-circuited SOA, because forward SOA without gate turn-off is limited by static latch-up whereas short-circuited SOA is limited by dynamic latch-up. Short-circuited SOA decreases as conduction time increases. This example is seen in Fig. 11 for 1200 V devices. Short-circuited SOA is a good practical estimation, because it includes both switching SOA and forward SOA, and because it gives underestimation if constant voltage source voltage is taken as drain voltage value, which actually
becomes greater than the constant voltage source voltage at the turn-off transient due to circuit stray inductance as seen in Fig. 10.

5. Conclusion

1800 V 10 A Bipolar-MOSFETs were developed based on two new technologies: Silicon Wafer Direct Bonding and a new junction termination technique. A high switching speed (0.45 μsec fall-time) and non-latch-up characteristics were successfully attained.

Acknowledgement

The authors thank Mr. Furukawa and Mr. Fukuda for fabricating SDB wafers for 1800 V devices.

References

[1] A. Nakagawa et al, 1984 Ext. Abs. 16th Conf. Solid-State Devices Mater., p.309.
[2] A. M. Goodman et al, 1983 IEEE IEDM Technical Dig. pp.79.
[3] M. F. Chang et al, 1983 IEEE IEDM Technical Dig. pp.83.
[4] A. Nakagawa et al, 1984 IEEE IEDM Technical Dig. pp.860.
[5] A. Nakagawa et al, 1985 IEEE IEDM Technical Dig. pp.150.
[6] K. Watanabe et al, Trans. IECE Japan, E69, 246 (1986)
[7] M. Shimbo et al, Ext. Abs. 169th Electrochem. Soc. Meeting. pp.337 (1986)
[8] A. Nakagawa et al, IEEE Electron Device Lett., EDL-6, 378 (1985)

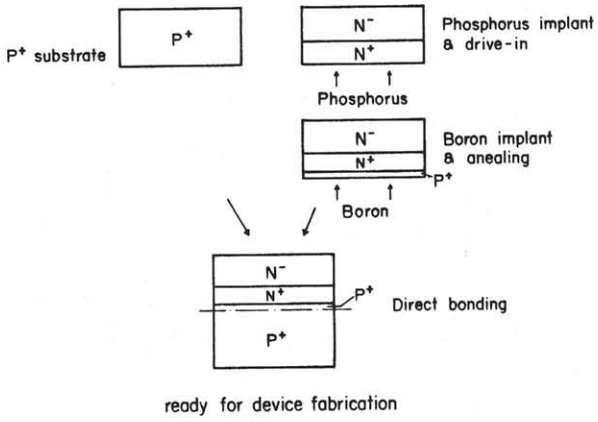

Fig. 1 Silicon wafer direct bonding process sequences

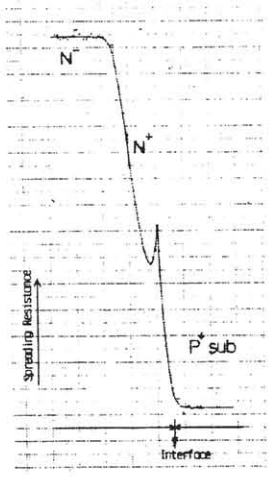

Fig. 2 Measured spreading resistance profile for $n^-/n^+/p^+$ structure fabricated by SDB

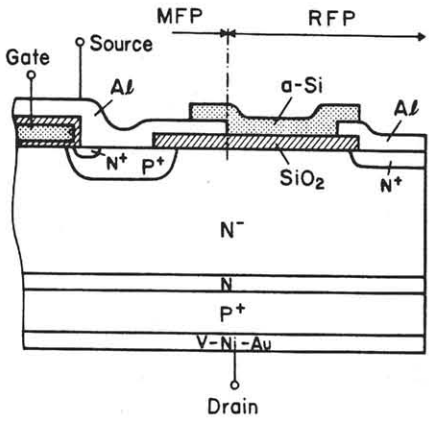

Fig. 3 Junction termination technique for 1800 V devices

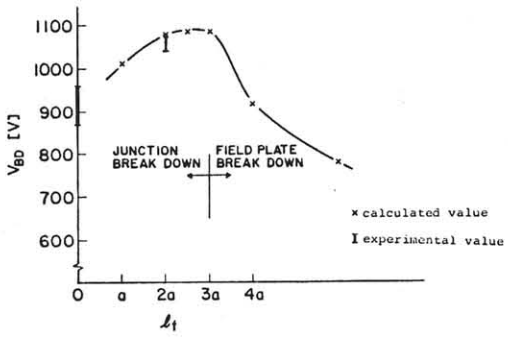

Fig. 4 Dependence of breakdown voltage on metal field plate length l_f.(Calculated values for a 1000V device)

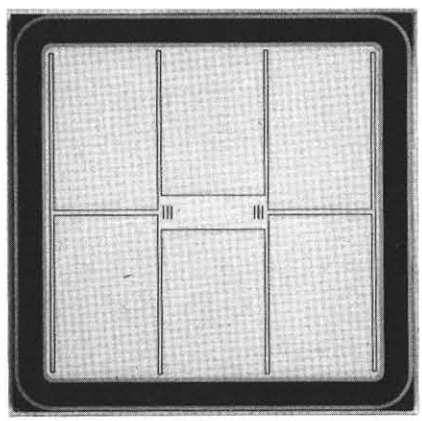

Fig. 5 1800 V 10 A device chip

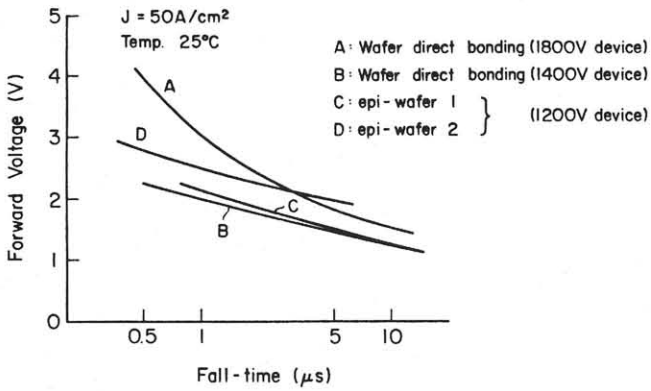

Fig. 6 Trade-off curves between forward voltage and fall-time

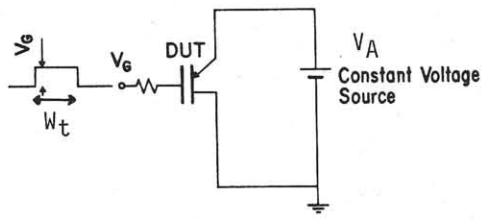

Fig. 9 Test circuit for short-circuited SOA measurement

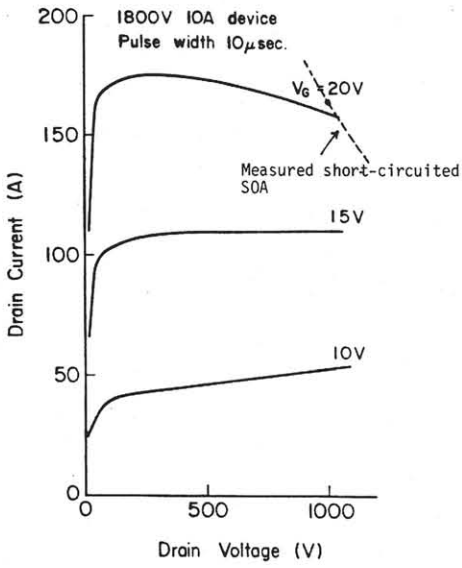

Fig. 7 High voltage high current saturation characteristics and Short-circuited SOA (broken line)

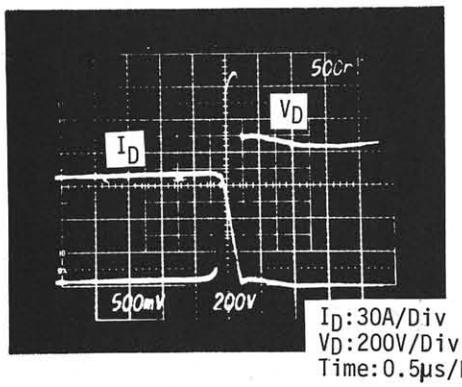

Fig. 8 Typical 100 A switching-off waveform

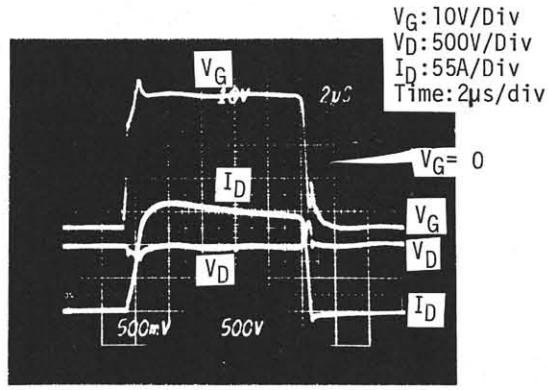

Fig. 10 Typical waveform for short-circuited SOA measurement.
Drain voltage is kept the same as constant voltage source voltage: V_A.

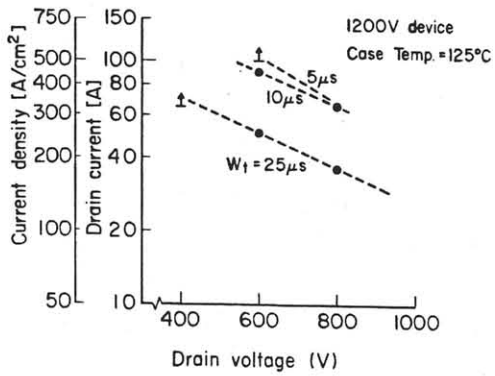

Fig. 11 Typical short-circuited SOA for 1200 V devices with conduction time W_t as a parameter