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A New Injection Suppression Structure for Conductivity Modulated Power MOSFETs

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A new device structure suited for suppression of the minority carrier injection in the conductivity modulated power MOSFET is presented. The new structure is featured by the presence of the n^+-ring region at the chip peripheral that is electrically connected to the bottom p^+-drain region. This permits the remarkable suppression of excessive carrier injection into the epitaxial-buffer region due to the lowered forward bias to the base of integral PNP transistor.

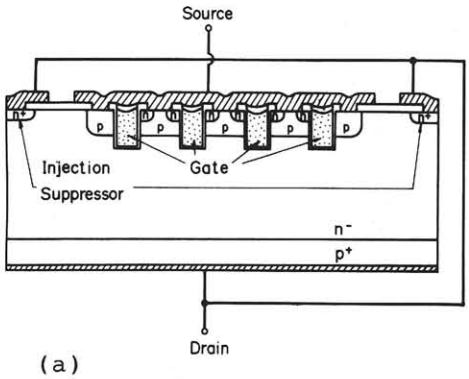
Experimentally fabricated device exhibited an improvement of the switching time by more than twice.

1. Introduction

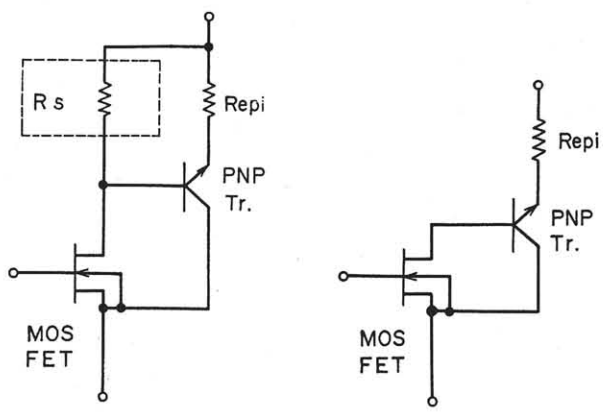
Recently, vertical power MOSFETs have been widely used in the power electronics field owing to fast switching capability and excellent thermal stability. The power MOSFET, however, possesses an inherent drawback that the current handling capability decreases as the breakdown voltage increases. Namely, the on-resistance increases proportionally to the 2.5 power of the breakdown voltage (1).

In order to overcome the above drawback a variety of new device structures called IGT(2), COMFET(3), and Bipolar-Mode MOSFET(4) have been developed by introducing a conductivity modulation effect in the epitaxial layer with high resistivity. Although the conductivity modulated MOSFET has an extremely low on-resistance and thereby a large current handling capability, it suffers from relatively poor switching performance and susceptibility of latching effect caused by uncontrollable excessive minority carrier injection.

In this paper, we demonstrate a new conductivity modulated MOSFET structure which permits remarkable suppression of minority carrier injection out of the bottom drain diode so as to improve the switching performance. The feature of the new structure is that the injection suppression ring is placed at the periphery of the chip and electrically connected to the bottom drain region in order to make short-circuit the injection diode.



(a)



New structure Conventional structure

(b)

Fig. 1 (a) A schematic cross-section of power MOSFET with new injection suppression structure, and (b) equivalent circuits for new and conventional conductivity modulated MOSFETs.

2. INJECTION SUPPRESSION STRUCTURE

A schematic cross-section of the new structure is shown in Fig.1 together with its equivalent circuit . Presence of the n+-ring having the same potential with that of p+-drain/emitter region allows lowering the forward biasing to the base of the integral PNP transistor so that the excessive carrier injection into the n--buffer region can be suppressed. The concept of the mechanism is illustrated in Fig. 2. Under the low drain voltage range where no hole injection occurs out of the p+-region , the electrons supplied from the sidewall channels flow to the n+-ring region through the n--buffer region. This means that the n+-ring region acts as a subsidiary drain with a large drain resistance Rs. As the drain bias increases, the voltage drop across Rs increases so that the hole injection out of the p+-drain/emitter region may occur as shown in the figure. The mechanism of the injection suppression are as follows. If the hole injection becomes large enough to recombine with the whole electrons supplied by the upper FET, the voltage drop across Rs begins to decrease, resulting in lowering the forward biasing the bottom drain diode. Consequently, the excessive carrier injection is suppressed with reduced minority carrier storage effect in switching operation. Another point to be noted is that the base and emitter region is short-circuited while the conventional conductivity modulated structure has an open-base structure. This is also advantageous in improving the switching performance.

3. DEVICE FABRICATION & ELECTRICAL CHARACTERISTICS

Experimental device were fabricated by using a Rectangular grooved MOSFET (RMOSFET(5)) structure which permits the lowest channel resistance per unit area among various power MOSFET structures.

The starting material used was an n-/p+ silicon epitaxial wafer with an epi resistivity and an thickness of 30 ohm・cm and 40 μm respectively. The process used was the conventional one with no life-time control. Boron and arsenic ions were implanted to form the p-body and n+-source regions. The n+-ring region, which is placed about 500 μm apart from active FET region, is formed simultaneously with the n+-source formation. Diffusion lengthes of the p-body and n+-source regions were 2.5 μm and 0.4 μm, respectively. Rectangular grooves with a spacing of 14 μm are engraved to a depth of 3.0 μm by using the RIE technique. Sputtered Al-Si-Cu ternary alloys were used for metalization.

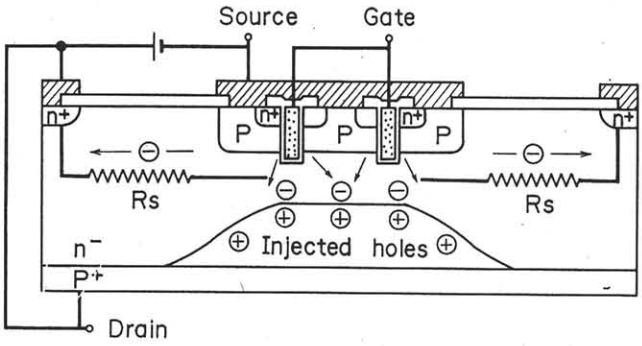


Fig. 2 Injection suppression mechanism.

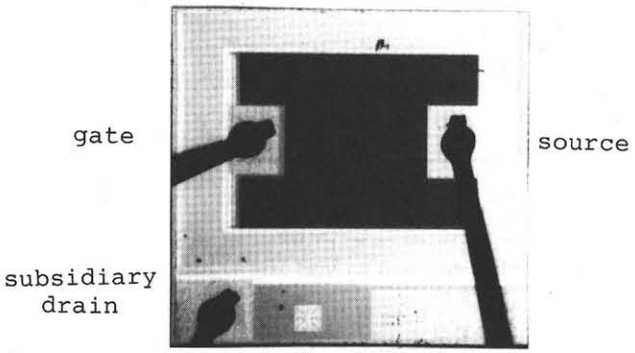


Fig. 3 Photomicrograph of fabricated chip.

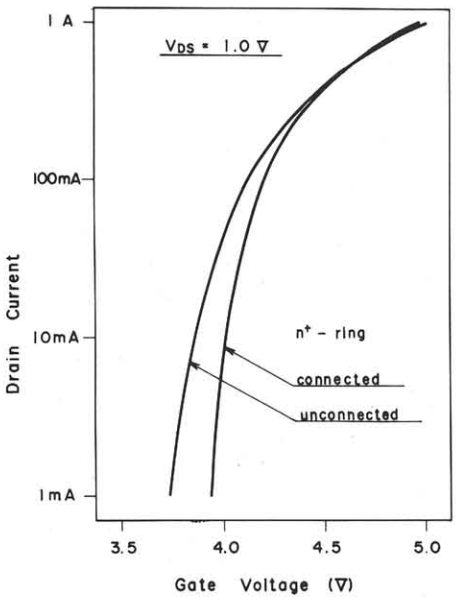
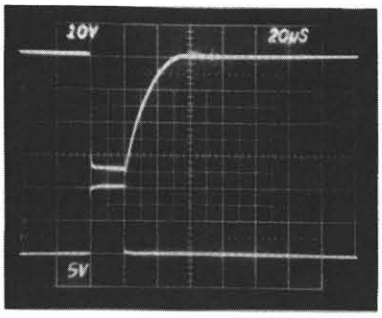


Fig. 4 Measured drain current as a function of gate voltage for two cases where n+-ring is electrically connected and unconnected to bottom p+-drain/emitter region.

(a)



(b)

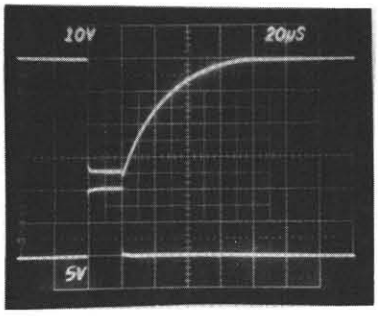


Fig. 5 Switching characteristics for two cases, (a) n+-ring is connected to bottom p+ region,and (b) n+-ring is unconnected to bottom p+-region.

The n+-ring region is electrically connected to the bottom p+-drain/emitter region by making use of external wire-bonding. Fig. 3 shows the chip photo-micrograph mounted on To-3 package.

The fabricated device has a breakdown voltage of 250V and an on-resistance of 0.35 ohm at a drain current of 2A. In Fig. 4, the drain current is plotted as a function of the gate voltage for two cases where n+-ring is electrically connected and unconnected to the bottom drain /emitter region. Note that unconnected case substantially corresponds to the conventional conductivity modulated MOSFET. It is seen that the drain current is decreased by more than one order of magnitude at the same gate bias condition. This is because that the hole-injection out of the bottom diode region is remarkably suppressed by reducing the potential difference between the emitter and base regions of the integral PNP transistor.

The switching characteristics are shown in Fig. 5 also for above two cases under the condition of drain current and voltage of 1A and 20V, respectively. It is seen that the switching time is improved by more than twice in the present new structure.

4. DISCUSSIONS

In order to investigate the detailed mechanism of the injection suppression for the new structure, two dimensional numerical analyses was performed for the region where injection suppression occurs. In the simulation, we used five electrodes n+-source, p-body, p+-drain /emitter, and n+-ring to be biased independently as shown in Fig. 6 . The currents which flow into four terminals except for the gate were calculated as a function of gate voltage under a condition that both of the p+-drain/emitter and n+-ring regions are biased to be +1.0V. The results are shown in Fig. 7 , where the solid lines denote the currents that go out from the n+-source region (Is+) and the p-body region (Ib+) and dotted line denote the currents that flow into the p+-drain/emitter region (Id-) and the n+-ring region (Ir-). In the figure, it is seen that in low gate-voltage range Ir- is equal to Is+ while in large gate-voltage range Id- is almost equal to Is+. This implies that the bipolar-mode operation (Conductivity Modulation) takes place above a certain gate voltage replacing the unipolar-mode one. It is also noted that that Id- exceeds Is+ in the high gate-voltage range. The difference between these currents attributed to the hole current flowing into the p-body region. The fact that ratio Ib+/Is+ obtained in the figure of as small as 30% indicates that hole-injection is well suppressed resulting in the remarkable improvement of the minority carrier storage effect(6). The hole distribution profile in this condition is shown in Fig. 8. It is seen that hole injection becomes smaller as the location far from the FET region due to the voltage drop by the internal resistance Rs.

5. CONCLUSION

It has been shown that the new injection suppression structure presented here is suited for improving the turn-off characteristics of conductivity modulated power MOSFETs. The experimentally fabricated device with the new structure exhibited an improvement of the switching performance by more than twice.

It is expected that the injection suppression structure with the use of conventional life-time control process may conduct to the further improvement of the switching performance.

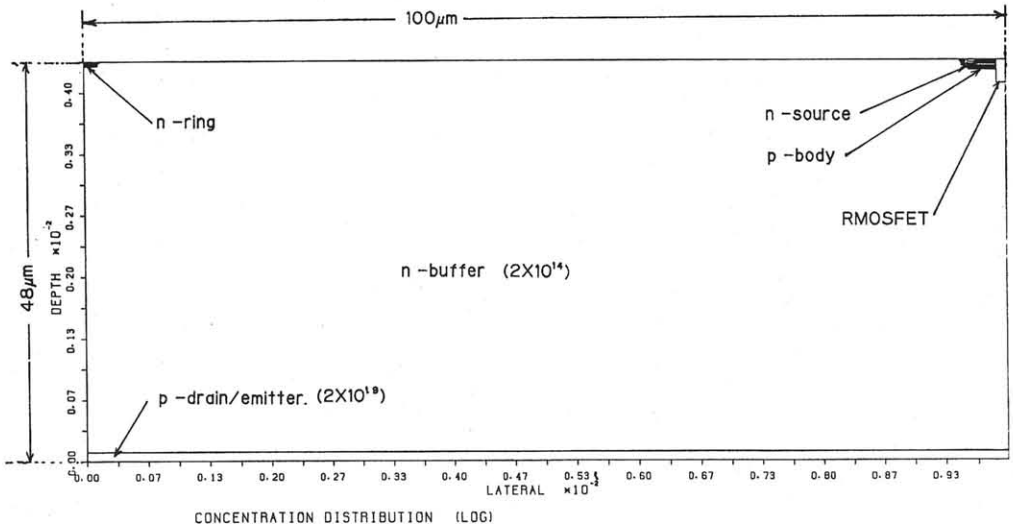


Fig. 6 Structure for 2-D numerical analysis.

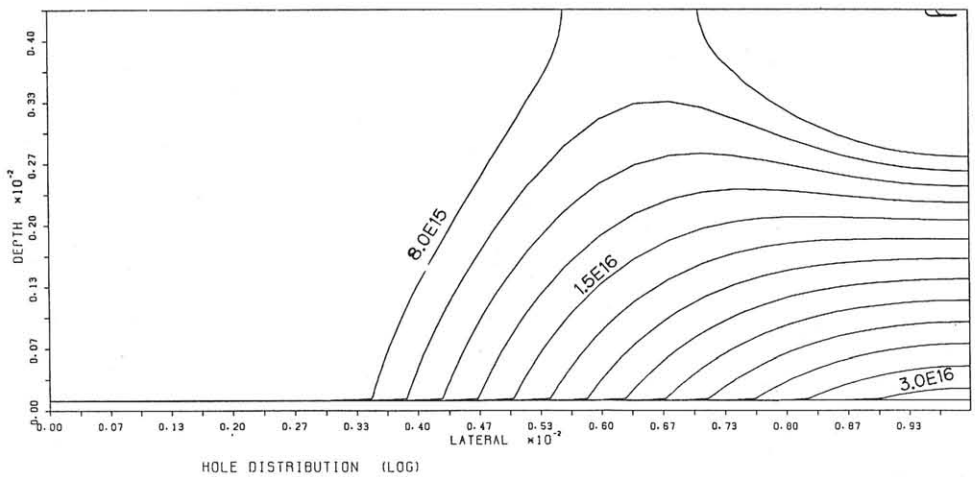


Fig. 8 Hole distribution profile under conditions of gate and source voltages of 5V and 1V, respectively.

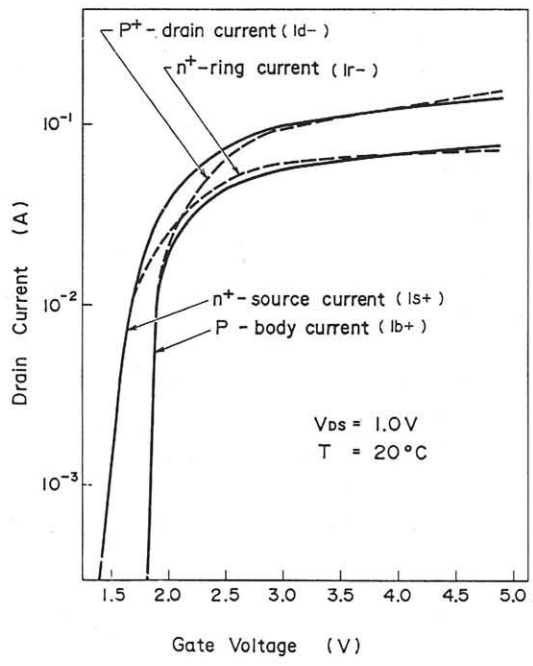


Fig. 7 Calculated current components, Is+, Ib+ , Ir-, and Id- as a function of gate voltage.

Acknowledgement

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REFERENCES

1. A. Tamer, et al, IEEE T-ED, vol ED-30, pp73-76, 83
2. B. J. Baliga, etal, IEDM Tech. Dig. 82, pp264-267
3. J. P. Russel, et al, IEEE EDL-4, pp63-66, 1984
4. A. Nakagawa, et al, ICSSDM Tech. Dig.84, pp309-312
5. D. Ueda, et al, IEEE T-ED, vol ED-32 no.1, pp2-6
6. D. S. Kuo, et al, IEEE EDL-6 no.5, pp211-214, 1985