

Inversion-type N-channel MOSFET Using Antiphase-domain Free Cubic-SiC Grown on Si(100)

K.Shibahara, T.Saito, S.Nishino* and H.Matsunami

Department of Electrical Engineering, Kyoto University,
Yoshidahonmachi, Sakyo, Kyoto, 606, Japan

We report the first success in fabrication of an inversion-type MOSFET of cubic-SiC grown on a Si(100) substrate. Cubic-SiC is a promising candidate for high temperature electronic devices because of its wide bandgap(2.2eV) and high electron mobility($1000\text{cm}^2/\text{Vsec}$). However, the cubic phase is stable at lower temperatures and growth of single crystals by ordinary sublimation has been difficult. We succeeded in heteroepitaxial growth of single crystalline cubic-SiC with a large area on a Si(100) substrate by introduction of carbonization process previous to CVD growth [1]. Carbonization is necessary to overcome the large lattice mismatch of 20% between SiC and Si.

Epitaxial growth of cubic-SiC by CVD was carried out in a horizontal quartz reaction tube using a $\text{SiH}_4\text{-C}_3\text{H}_8\text{-H}_2$ system. Carbonization of a Si substrate and CVD growth were carried out in turn after gaseous HCl etching.

Figure 1(a) shows a Nomarski microphotograph of the grown layer on a (100) well oriented Si substrate. Texture-like morphology which originates from antiphase domains(APD) is observed. To realize active devices APD must be eliminated. By inclining a substrate towards (011) an APD free grown layer was obtained. Figure 1(b) shows surface morphology of the APD free grown layer. Inclining towards other direction resulted in APD, which was clarified by the growth on a spherically polished Si(100) substrate.

We fabricated an inversion-type MOSFET on the APD free grown layer. Figure 2 shows the structure of MOSFETs. MOSFETs were fabricated on B-doped p-SiC($d \sim 2\mu\text{m}$, $p \sim 10^{15}\text{cm}^{-3}$) grown on undoped n-SiC($d \sim 7\mu\text{m}$, $n \sim 10^{17}\text{cm}^{-3}$). Source and drain were formed by two step ion implantation of P^+ . The first implantation was at a dose of $1 \times 10^{15}\text{cm}^{-2}$ with an ion energy of 100KeV, and the second was at $3 \times 10^{14}\text{cm}^{-2}$ with 25KeV. Annealing after implantation was carried out in an IR radiative heating furnace in Ar atmosphere at 1080°C for 1hr. SiO_2 as a gate oxide of about 60nm was obtained by thermal oxidation of SiC at 1050°C using dry oxygen for 6hrs

*Present address: Kyoto Inst. of Technol., Matsugasaki, Sakyo, Kyoto, Japan

based on our previous results [2]. The gate length and width are $20\mu\text{m}$ and $500\mu\text{m}$, respectively. Figure 3 shows current-voltage characteristics of a MOSFET. The action of inversion-type MOSFETs was achieved for the first time. Leak current between source and gate was less than $1\mu\text{A}$ for the gate bias of $\pm 10\text{V}$. Since any processes for fabrication are not optimized, the FET characteristics can be improved much more.

References

[1] S.Nishino et al., Late News Abst. 16th Int. Conf. SSDM, 1984, p8.
 [2] K.Shibahara et al., Jpn. J. Appl. Phys. 23(1984)L862.

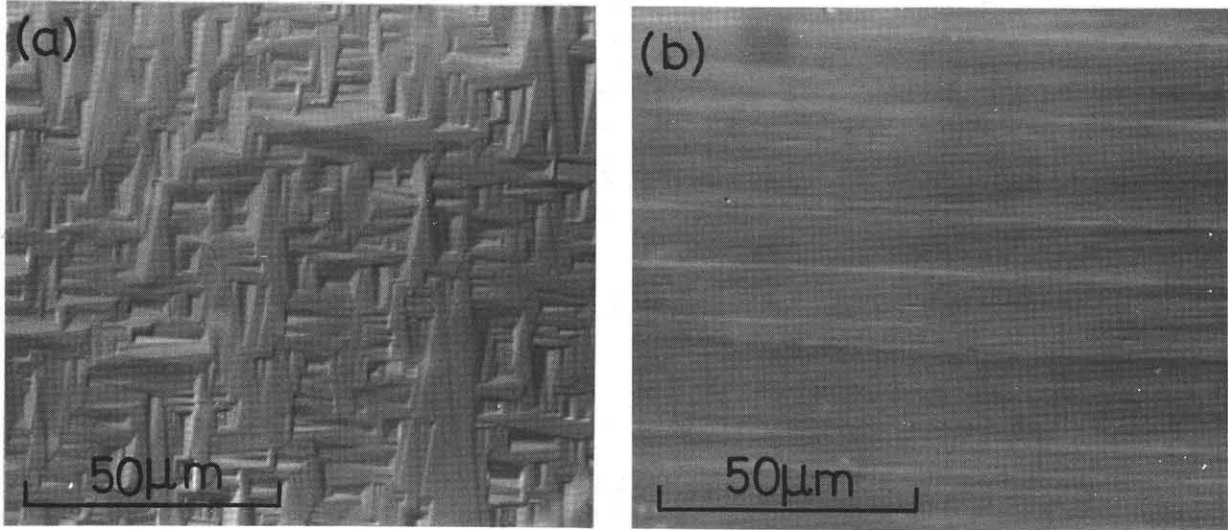


Fig.1 Nomarski microphotograph of surface morphology of the grown layer (a) on the (100) well oriented substrate and (b) on the substrate tilted towards (011).

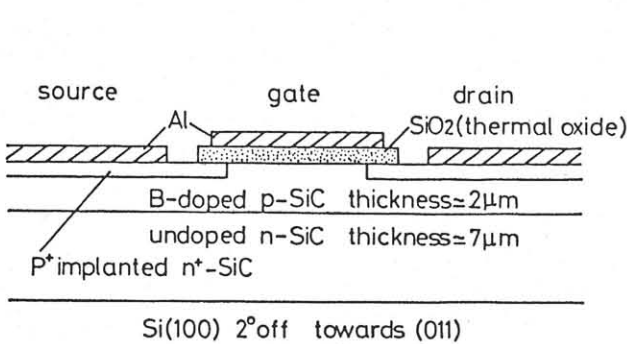


Fig.2 The structure of MOSFETs

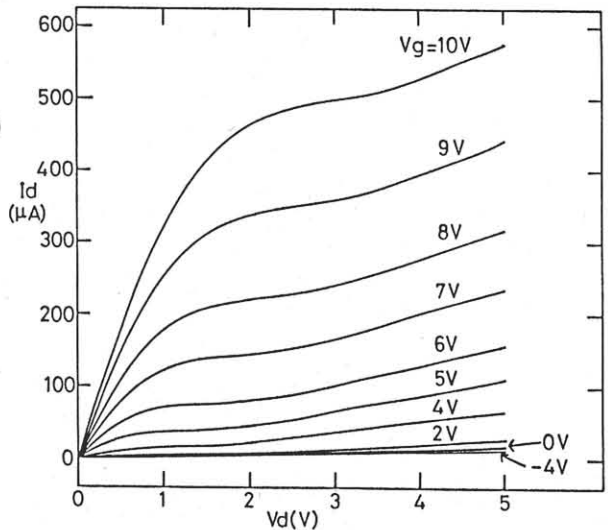


Fig.3 Current-voltage characteristics of a MOSFET