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Invited

Renaissance of Bipolar Technology

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Current trends in bipolar technology are discussed. It will be demonstrated that bipolar technology is getting new powerful momentum based on i) improvements in technology synergetically using MOS techniques, ii) new concepts such as self aligned structures or polysilicon emitters.
Exploiting these innovations is shown to drastically reduce parasitics and device dimensions, thus considerably extending the domain of bipolar technology towards high speed as well as high complexity systems.

1. Introduction

Vivid competition of bipolar and MOS technology exists for more than 15 years. Bipolar's end has been predicted regularly, however, it is still strong in business. Moreover it recently demonstrates new powerful momentum most likely leading to a larger share in future VLSI business than predicted before.

The real unique bipolar advantages havn't changed. They are still

- extremely high intrinsic speed ($\tau_d \leq 30$ps),
- extremely high driving capacity (transconductance g_m (Fig. 1)),
- extremely good threshold control $\Delta V_{BE} \approx 5$mV.

The new impulse for bipolars' therefore originates from different reasoning. It is based on

- improvements in bipolar technology synergetically using MOS techniques (poly-Si, silicides, salicides, trenches etc.),
- improvements in bipolar technology by using self alignment concepts (emitter to base, base to collector and isolation),
- a smaller increase in process complexity (e.g. 13 masks including 3 layers of metal plus passivation) compared to its major rival CMOS,

all of them resulting in drastically better yield as well as performance data.

2. Advanced Bipolar Technology

2.1 Self aligned structures /1, 2/

Self aligned structures require less complex processing (independent of lithography) and yield reduced devices dimensions and thus smaller parasitic capacitances. The most drastic effect is obtained by means of E/B self alignment.

- C_{BC} can be reduced by a factor of 5 as compared to a conventional process (2 /um lithography)

- R_B can be reduced by a factor of 2 to 5, depending on the poly-Si emitter effect used.

E/B self alignment requires careful optimization of the doping profiles within the E/B isolation region, because the heavily doped regions underneath the spacer oxides (Fig. 2) limit the breakdown voltage basically by tunneling effects. This finally leads to a trade off between switching speed desired and breakdown voltage required.

E/B to isolation self alignment allows to reduce drastically the C_{BC} capacitance, however, too small base contacting areas will override the effect on switching performance by increasing the base contact resistance. Careful optimization is required there too.

2.2 Poly-Si Emitter effect

Emitter junctions shallower than the hole diffusion length ($L_p(N_e = 2 \cdot 10^{20}\ cm^{-3}) \approx 200$ nm) become transparent to holes. In the case of metal contacting possible spiking of the metal results in high base currents and - what is worse - in an extremely poor process controllability.

The urgent need for new emitter contacting schemes with reduced interface recombination rates led to the discovery of the poly-Si emitter, which has been subject to a large number of investigations, all of them showing substantial increase in current gain.

The origins of this improvements hypothetically result from the unique features of the poly-mono interface and/or of the conductivity features of the poly-Si itself /4, 5/. Experiments give proof to both theories depending on the processing chosen.

Interfacial oxides (thermally grown, chemically, $d_{SiO_2} \approx$ 15-20 Å) result in:

- very low base currents (current gain 5-15 times larger than Al contact),
- difficult I_C controllability,
- large R_E.

Base currents and depending on the thickness of the oxide also collector currents are controlled by tunneling mechanisms (Fig. 3).

No or very thin interfacial oxides ($d_{SiO_2} \approx$ 0-10 Å) lead to transistors with

- ideal current characteristics,
- small but controllable emitter efficiency increase,
- the problem of epitaxial realignment of poly-Si.

In this case we have experimental proof /6/ that

- the base current is not determined by hole transport within the bulk of the poly-Si layer (Fig. 4),
- the reduced base current and enhanced current gain is caused by a barrier action of the poly/mono interface which is defined extending up to 400 Å into the poly-Si.

As a figure of merit for the effectiveness of the emitter contacting an effective recombination velocity S_{eff} at the poly-mono interface is introduced (Fig. 5). This parameter integrally describes recombination and transport phenomena within the poly-Si and the poly/mono interface and easily can be determined experimentally.

2.3 Resistances

A current gain of 100 is sufficient as well as desirable for ECL applications. The improved higher efficiency of the poly-Si emitter therefore can advantegeously be used to increase the active base doping thus drastically reducing base resistance.

The external base resistance is most conveniently reduced by using silicides as base contacts.

2.4 Capacitances

2.4.1 Base-Emitter Capacitance

Textbook information often is misleading when the effect of increased base doping on E/B junction capacitance has to be estimated for ECL techniques. For high forward injection as used in digital applications the measurement of junction capacitances is impracticable due to the high current densities. To model the effect of current on the capacitance, a diffusion capacitance is usually added to the junction capacitance. Both, however, neglect the influence of mobile carriers within the internal space charge layer, which becomes predominant in the case of heavily forward-biased pn junctions as recent results have shown /3/.

These charges decrease with increasing doping levels as indicated by first-order reasoning ($Q \sim 1/N$) and by complete numerical calculations of the complex situation (Figure 6). For digital applications, increased base doping will therefore not in any case result in higher E/B junction capacitance. Thus the integral emitter-base time constant, as the product of capacitance and base resistance, derives full benefit from the reduced base resistance and reads about $\tau_{BE} \approx 6$ ps for an emitter area of $A_E = 1\ \mu m \times 2\ \mu m$.

2.4.2 Base-Collector Capacitance

Numerical device modeling has similarly been used to simulate the effective base-collector (BC) capacitance and to determine the proper epitaxial doping level for self-aligned transistors which differs from that of conventional transistors. This is not apparent at first glance because the BC capacitance of conventional transistors is basically a reverse-biased junction capacitance, only a small portion of which is flooded with collector current. Increased epitaxial doping is therefore not advisable because it leads to increased capacitance.

The situation is different for self-aligned structures, where a substantial portion of the BC capacitance is flooded with collector current. Within this portion of the capacitance minority carrier storage plays a major role. The stored charges decrease with increasing epi-doping. This leads to a BC capacitance minimum as a function of epi-doping. Complete numerical calculations using MEDUSA /7/ reveal the existence of this minimum at a doping level of about $2 \cdot 10^{16}$ cm^{-3} (Fig. 7) for 2 µm lithography.

2.5 Isolation

On top of the conventional junction isolation two different structures for oxide isolation are being used, which can be characterized by:

i) LOCOS type isolation scheme;
   - well established technique, for about 10 years in production,
   - advanced processes with planar topography and small windages being developed (SPOT /8/, SWAMI /9/, OXIS /10/),
   - relatively low crystal defect density ($\rho_{defect} \leq 10^3$ cm^{-2}),

ii) trench isolation scheme;
   - very small devices can be devised yielding high integration density,
   - very small C_{CS} and R_C obtainable yielding improved performance ($\tau_d \leq 30$ ps),

- synergetic processing taking advantage of the ongoing developments of the DRAM trench cell,
- complex processing for in-trench substrate contact needed.

The trench isolation certainly offers better possibilities for advanced structures. Very impressive bipolar processes with trench isolation have been proposed. However, it is still an open question whether trench isolation will give sufficient yield in production.

2.6 Performance

Performance data are impressively being demonstrated by the power delay products achieved in the last years (Fig. 8) but even more relevant for the system engineer by a diagram showing the system speed actually achieved by different technologies as a function of chip complexity (Fig. 9). With improved yield bipolar technology attacks the MOS side whereas with improved performance it maintains its good situation at the III-V side. Furthermore it demonstrates which applications drive which technology.

3. Technology Trends and consequences

New self aligning concepts and the use of clever emitter contacting schemes (poly-Si emitter effects) overcome the limitations of conventional bipolar transistors, so that at present no severe limitations for further improvement are in sight. However, the trade off between performance and breakdown voltage has to be met by reducing the breakdown voltage requirements.

Drastic further improvements of processing and performance are to be expected by using

1. new materials as diffusion sources, for low resistance contacting and especially for the metallization system (becoming more and more of primary concern for bipolar and CMOS);

2. new processing techniques like advanced lithography and especially rapid thermal annealing;

3. new device structures like better self aligning schemes (e.g. salicides) and hetero emitter structures.

Even more important however is to realize a general trend which can be observed since quite some time and which will become more and more the major driving force for future bipolar work. I would like to call this trend MOS-BIPOLAR TECHNOLOGY CONVERGENCE. Such a convergence is being pushed by both technical as well as economical reasons. It has been observed by most processing engineers as a general feeling, it can however be described quantitatively as seen in Fig. 1. The extrapolation into the early 90's for MOS using more bipolar knowhow (epitaxy, low resistive contacting, multilevel metallization) and bipolar using more MOS techniques (silicides, trenches, etc.) is justified by the synergetical use of process developments and therefore finally by the drastic savings in development as well as prodction costs. As a last consequence there will no longer exist an urgent need for seperate development lines and even more the capacity of production lines can be used much more economically.

Last not least this general trend will make an old designer's dream come true, the combination of CMOS- and BIPOLAR-transistors on chip combining the inherent advantages of both technologies. Due to the convergence of technology the overhead in processing will be quite limited (about 3 masks and 15 % to 20 % more processing steps). The advantages of such a technology will enable VLSI and ULSI chips with both ultra high system complexity and ultra high system speed.

A large spectrum of applications ranging from fast real time signal processing via large data processing units to advanced communication systems is driving this technology approach.

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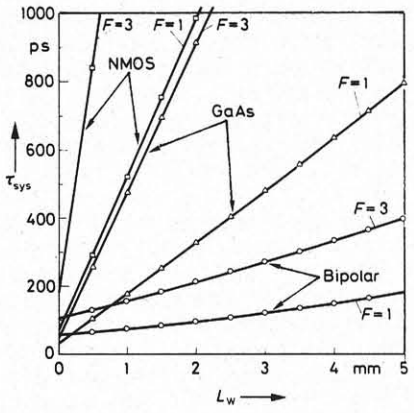

Fig. 1: System delay time τ_{SYS} as a function of the wiring length L_W and fan-in/fan-out. Design rules and transconductance for bipolar, GaAs and MOS transistors are 1.0 µm, 0,2 µm, 0,2 µm and 6,6 mS, 0,93 mS, 0,43 mS respectively. Wiring parameters: C_W = 0,15 pF/mm, W = 1,5 µm.

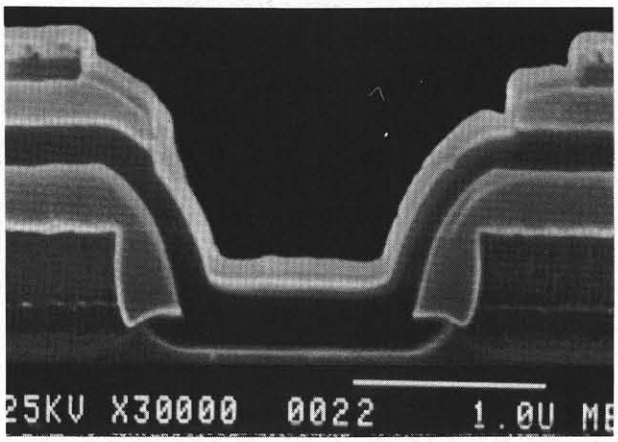

Fig. 2: SEM cross section of self aligned E/B structure

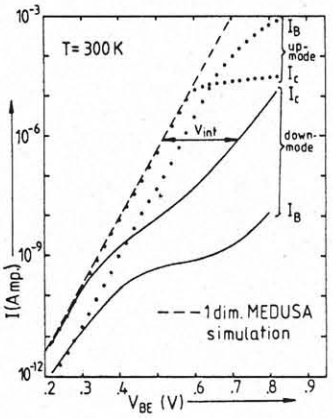

Fig. 3: I_C and I_B versus V_{BE} for normal (downward) and inverse (upward) operation

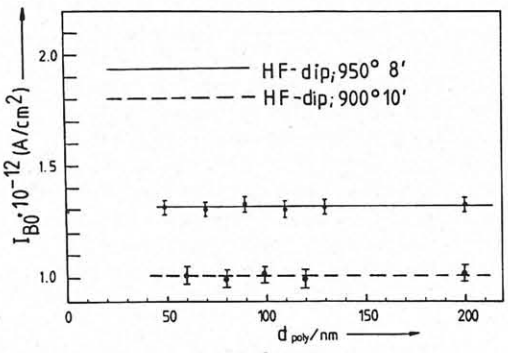

Fig. 4: Base saturation current independence on poly-Si thickness ($d_p \geq 50$ nm) for HF-dip devices.

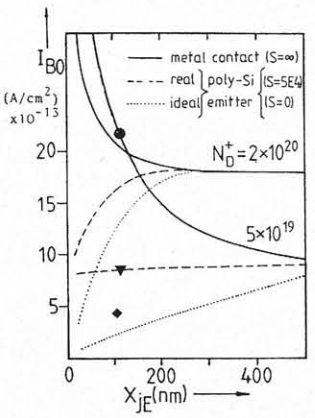

Fig. 5: Simulation showing the impact of various device parameters on the base current of poly-Si emitters. Experimental data for the metal contacted device (●), HF-dip (▼) and RCA cleaned (◆) interface are also included.

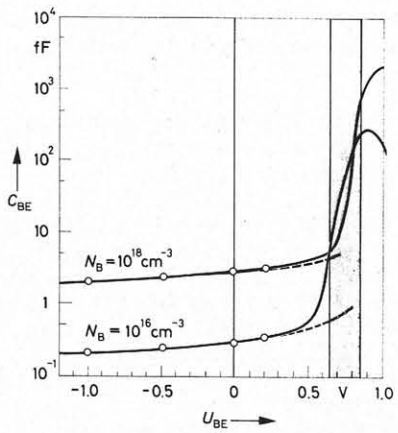

Fig. 6: Emitter-base capacitance C_{BE} as a function of U_{BE} (simulation). The rings indicate measured data.

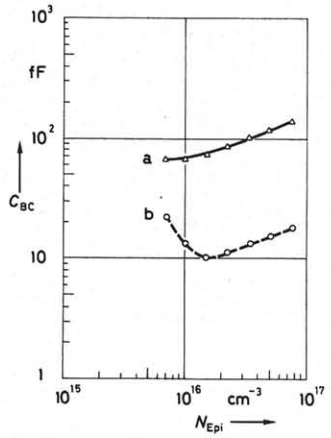

Fig. 7: Base-collector capacitance C_{BC} as a function of the epitaxial doping N_{Epi} (simulation) for a conventional (a) and a self-aligned transistor (b). A_E = 2 /um x 4 /um.

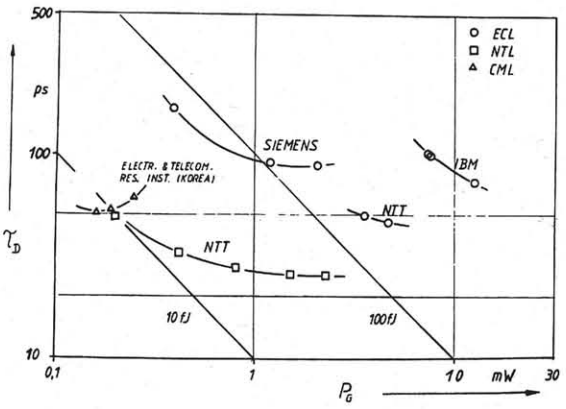

Fig. 8: Gate delay versus power characteristics /1, 11, 12/.

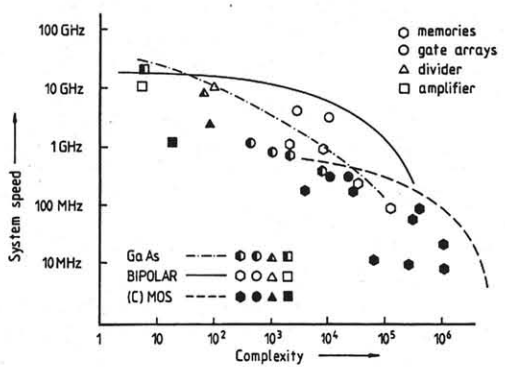

Fig. 9: Gate delay as a function of complexity

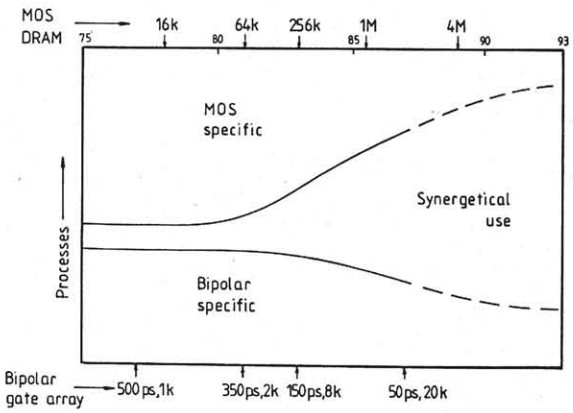

Fig. 10: MOS-Bipolar Technology convergence