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A 1.0 ns 5-Kbit ECL RAM

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ABSTRACT

A bipolar 512×10-Bit ECL RAM with an access time of 1.0 ns and a power dissipation of 2.4 Watts, achieving an access time power/bit product of 0.48 pJ/bit, has been developed. The RAM was fabricated using an advanced bipolar technology featuring poly-base self-alignment, poly-emitter shallow profile, and silicon-filled trench isolation with a minimum mask dimension of 1.2 μm. A Schottky-clamped multi-emitter cell with a cell size of 760 μm^2 is obtained as a result of compact cell layout and the use of 1.2 μm trench isolation.

I. INTRODUCTION

High speed ECL RAM, used in cache memories or control store, is one of the most crucial elements in determining the performance of mainframe computer systems. As a result of recent progress in circuit innovation and advancement in process technology such as smaller lithography dimensions, improved isolation and shallow profile, 4-KBit ECL RAMs with sub-5 nanosecond access time have been realized [1] [2] [3] [4]. With the use of advanced polysilicon self-alignment scheme, a 1-KBit ECL RAM with 0.85 ns access time and a 4-KBit ECL RAM with 1.1 ns access time have been reported [5] [6]. These high speed 1K - 4K bit ECL RAMs are typically designed with Schottky-clamped multi-emitter cell to achieve fast read/write operation. Despite the use of lithography level around 1.0 μm, the memory cell size has been limited to around 1000 μm^2 or above [1-6]. This paper describes a 512×10-Bit RAM using 1.2 μm double-poly self-aligned process [7] in conjunction with silicon-filled trench isolation. An access time of 1.0 ns is achieved with a power dissipation of 2.4 Watt, featuring an access time power/bit product of 0.48 pJ/bit. Compact cell layout, in conjunction with the use of 1.2 μm wide trench isolation, results in a cell size of 760 μm^2. The major feature of the design and fabrication technology are given below.

II. FABRICATION TECHNOLOGY

The process employed trench isolation with double layer metallization. Typical process parameters are shown in Table I. The RAM is built on an 0.4 Ω-cm n-type epitaxial layer of 0.7 μm flat zone with an optical 10X stepper at a minimum mask dimension of 1.2 μm. A double-poly self-aligned process which reduces the base-emitter contact spacing and results in very small base-collector capacitance and collector-substrate capacitance is used. The 1.2 μm deep-trench isolation is filled with selective-epi-silicon. The insulating top cap of the trench isolation is formed using a self-aligned process by thermally oxidizing the silicon trench without any additional masking step, thus making it suitable for dense memory applications. Details of this device technology have been described elsewhere [8].

The contact hole for the Schottky anode is opened at the contact level together with the contact hole to the p^+ polysilicon base by reactive-ion etch. The same PtSi metallurgy that is used for the Schottky contact is also used for ohmic contacts to the p^+ polysilicon base and n^+ polysilicon emitter. The inter-metal dielectric consists of a composite layer of LPCVD nitride and polyimide.

III. CIRCUIT DESIGN

A standard Schottky-clamped multi-emitter memory cell is used for fast read/write operation. The schematics and microphotograph of the cell are shown in Fig. 1. The load resistor is 6 KΩ while the drain line current equalizing resistor is 2 KΩ. The standby current and read/write current are 50 μA/cell and 0.87 mA, respectively. A minimum size emitter - 1.2 × 2.4 μm^2 (mask dimensions) - is used for the drain line transistors in the cell to reduce the capacitance while a slightly larger emitter - 1.6 × 2.4 μm^2 - is used for the bit line transistors in the cell to conduct the large read/write current. A cross section of the memory cell is illustrated in Fig. 2. To increase the hold voltage of the selected cell, high barrier PtSi Schottky diodes (Φ_B = 0.85 eV) with an anode area of 40 μm^2 are used. As a result, a collector node voltage difference of 600 mV is obtained for the selected cell. The Schottky diode has a self-aligned guard ring [9] formed at the same time as the extrinsic base region of the n-p-n transistor. The guard ring is connected to the anode via the first metal and hence its capacitance adds to that of the Schottky diode. This capacitance actually reduces the access time and improves the soft error immunity as it increases the capacitance at the collector nodes of the cell transistors and helps to charge up the base nodes faster during the switching transient. Notice that the p^+-poly contacts for the cell transistors and the guard ring of the Schottky diode also serve as the contacts for the load resistor. This compact cell layout, together with the use of 1.2 μm silicon-filled trench isolation, results in a cell size of 760 μm^2 which is among the smallest for designs in the 1-3 ns access time range [1-6] [10-12].

Large transistors with long and narrow multi-emitter stripes are used extensively in the peripheral circuits to reduce the base resistances for high speed operation. Extensive simulations indicate that the use of long and narrow multi-emitter stripes improves the performance by about 15-20 % as compared with a non-optimized design where single wider emitters are used. Current mirrors are used to source the cell standby currents as well as the peripheral circuits to save the voltage drop across the emitter resistor in a current source such that the whole array can operate at a total voltage of 3.6 volts.

A schematic diagram of the RAM is shown in Fig. 3. The decoder consists of a multi-emitter AND gate with a feedback resistor between the collector and the base to improve the DC current balance, transient speed, and to equalize the current distribution to the AND gates from a single address buffer [13]. A word line swing of 0.85 V is chosen to realize a maximum

speed while avoiding inadvertent "write" into the unselected cell. To assure that the de-selected word line be de-selected before the selected word line is selected, small resistance values are used for the word line discharging resistors. (0.1 KΩ and 0.2 KΩ for R_3 and R_4 in Fig. 3, respectively)

The sense amplifier reference voltage is derived from a circuit which is a replica of a selected half-cell. The base and emitter of the drain line transistor in the half-cell are connected together since it is supposed to conduct only the small standby current. The emitter of the bit line transistor in the half-cell is connected to a current source such that a current equal to the read/write current would flow through this transistor to produce the same voltage drop across the Schottky diode and load resistor as in a selected cell. The decoder outputs and the sense amplifier reference circuit are then clamped by a common circuit so as to achieve proper word line swing and to assure good tracking between the sense amplifier reference voltage and the voltages at the collector nodes of the cell transistors.

Instead of an emitter follower output driver with a passive pull-down resistor which may introduce a prohibitively long RC delay when the output changes from the high to the low state, a totem-pole power-driver is used such that we have similar access times for both transitions under heavily loaded conditions owing to the active pull-up and pull-down configuration.

IV. CHARACTERISTICS OF THE 5-KBit RAM

The RAM is designed to have an organization of 512 words by 10 bits. Fig. 4 shows the block diagram of the RAM which consists of two blocks of 512×5-Bit memory arrays with the word line decoders placed in between to reduce the RC delay due to the word line. Separate emitter follower word line driver is used to drive each of the 512×5-Bit block. Since the word line driver has to drive the 5 selected bit line pairs with 0.87 mA each and to supply the standby currents to the unselected cells in the same word line as well as the word line discharging resistors (total load on the selected word line driver = 15.6 mA), a large emitter area of $10\times(1.2\times8.4)$ μm^2 is used. The word lines are placed as first metal with a width of 12.2 μm and run horizontally across the array. The bit lines are placed as second metal and run vertically. The directions of the first and second metals are interchanged in the peripherals for wiring consideration. The peripheral circuits are laid out by first placing all the wiring tracks available and then fitting the circuits into these wiring tracks. A first metal of 2 μm line width / 2 μm spacing and a second metal of 2.6 μm line width / 2.6 μm spacing are used to achieve a chip size of 3.4 mm × 4.4 mm.

Simulated internal waveforms under an output loading of 3.5 pF are shown in Fig. 5. In spite of the fast rise time for the selected word line, a minimum cell hold voltage of 250 mV is maintained. The total delay from the word address input to the data output is 1.1 ns which agrees well with measured results.

A microphotograph of the 5-KBit RAM is shown in Fig. 6. The address input and data output waveforms are shown in Fig. 7. The read access time of the 5-KBit RAM is 1.0 ns at a power dissipation of 2.4 Watt. The figure of merit defined as the access time power/bit product is 0.48 pJ/bit. The main feature of the RAM are listed in Table II.

V. CONCLUSIONS

This paper describes a 5-KBit RAM using 1.2 μm double-poly self-aligned process and silicon-filled trench isolation. Compact cell layout, combined with trench isolation, results in a cell size of 760 μm^2. A 5-KBit RAM with an access time of 1.0 ns at a power dissipation of 2.4 Watt is realized in a chip area of 3.4 mm × 4.4 mm.

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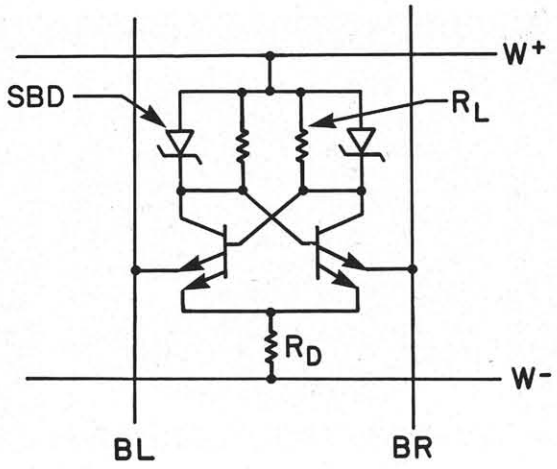
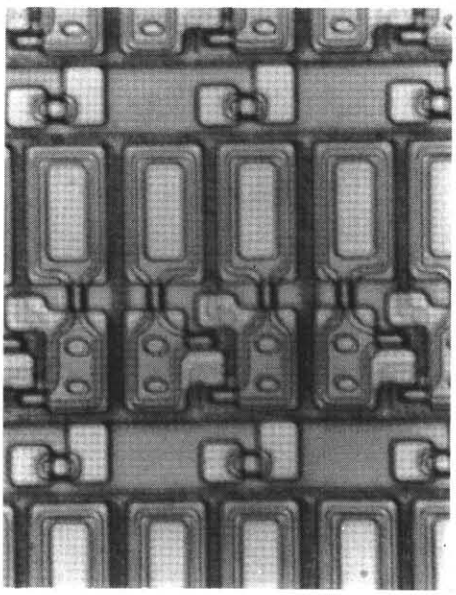


(a)



(b)

Fig. 1. (a) Schematics and (b) microphotograph of the Schottky-clamped multi-emitter ECL RAM cell.

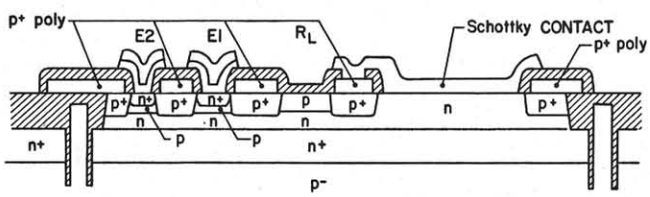


Fig. 2. Cross sectional view of the RAM cell.

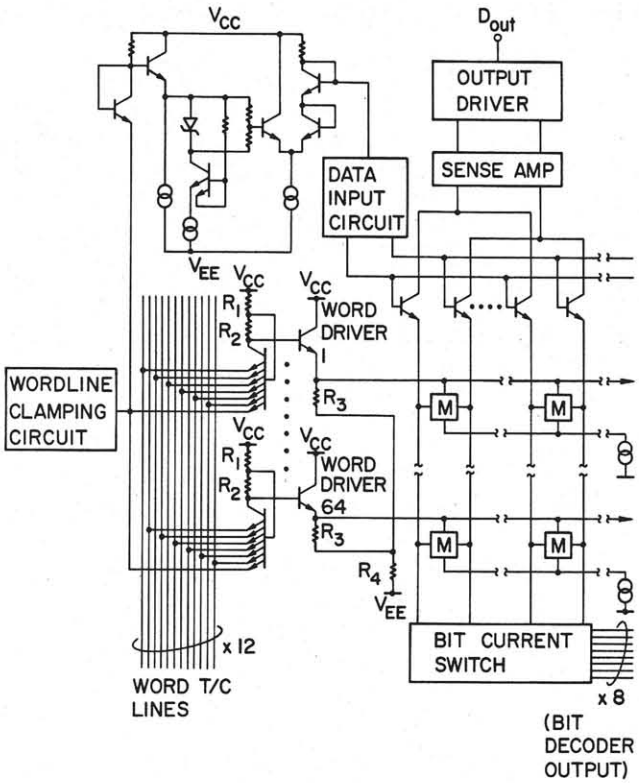


Fig. 3 Schematic diagram of the 5-KBit RAM.

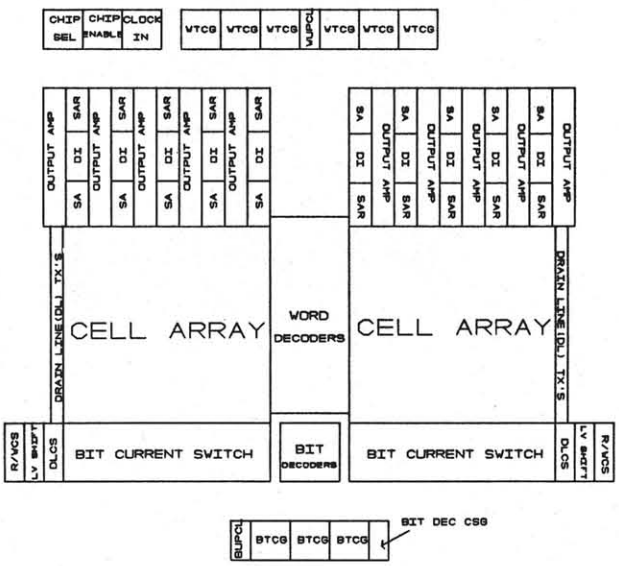


Fig. 4. Block diagram of the 5-KBit RAM.

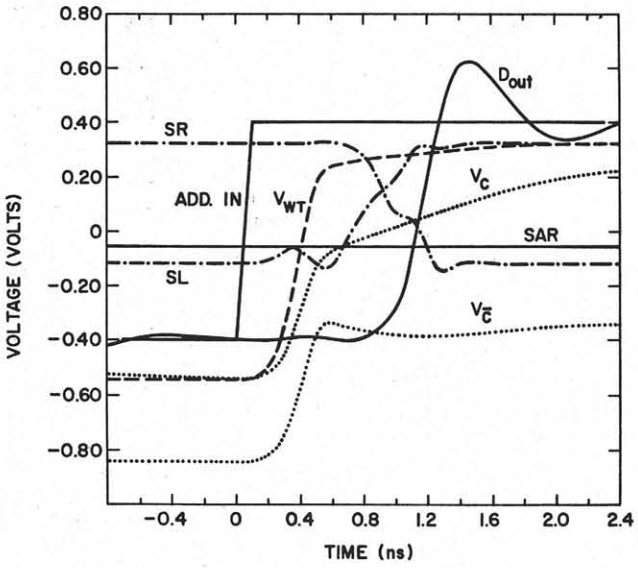


Fig. 5 Simulated internal waveforms of the 5-KBit RAM circuits.

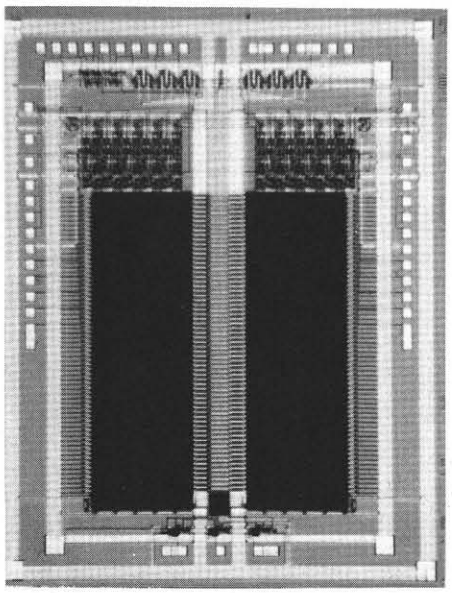


Fig. 6. Microphotograph of a 5-KBit RAM.

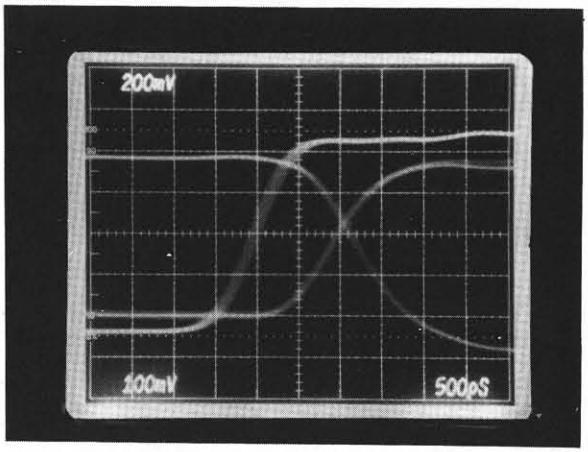


Fig. 7. Read access waveforms of the 5-KBit RAM.

TABLE I
TYPICAL PROCESS PARAMETERS

Epitaxial Layer Thickness	0.7 μm
Epitaxial Layer Resistivity	0.4 Ω-cm
Isolation	1.2 μm Trench & ROX
Minimum Emitter	1.2 μm x 2.4 μm
First Metal Pitch	4.0 μm
Minimum Via Size	2 μm x 2 μm
Second Metal Pitch	5.2 μm

TABLE II
CHARACTERISTICS OF THE 5-KBit RAM

Address Acess Time	1.0 nS
Organization	512 word x 10 bits
I/O Level	$\pm$0.4 V
Power Dissipation	2.4 W
Power Supply	3.6 V (Total)
Cell Size	20 μm x 38 μm
Chip Size	3.4 mm x 4.4 mm