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A Bipolar Gbit/s 8×8 bit S/P, P/S Converter LSI

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A Si bipolar very high-speed 8-channel x 8-bit Serial/Parallel and Parallel/Serial conversion LSI (SPPS-LSI), having 1.5 Gb/s throughput is developed for high-speed digital communication systems. To achieve high performance, a novel data conversion method is adopted. Furthermore, by applying a sophisticated circuit design and SST-1A process technology, a high-speed and low-power LSI is achieved with small chip size.

1. Introduction

Future very high-speed digital time-division data exchange systems will require very high-speed logic LSIs. The Serial/Parallel,Parallel/Serial conversion LSI (SPPS-LSI) is one of the key devices in this system. It converts serial input data streams into parallel output data streams, and vice versa. In this paper, a bipolar Gb/s 8 x 8 bit SPPS-LSI operating up to 1.5 Gb/s is described. This high performance is achieved using the following ;

(1) a novel conversion method,

(2) sophisticated circuit design, and

(3) Super Self-aligned process Technology (SST-1A).

2. Novel conversion method

The SPPS-LSI converts sequential 8 bit data from 8 input channels into 8 new output data sequences, as shown in Fig. 1. In conventional digital exchange systems, the SPPS-LSI is composed of shift registers and selectors, as shown in Fig. 2 [1]. The critical path of this LSI is data transmission through shift register, 8:1 selector, and D-type Flip-Flop (D-F/F). An 8:1 selector circuit is conventionally composed of seven 2:1 selectors. Therefore, critical path delay becomes an obstacle to performance improvement.

To achieve a high-speed and low-power LSI with small chip size, a novel conversion concept using a shift register array is proposed. To explain the operation

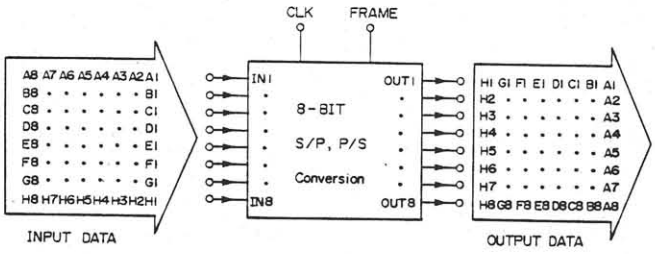

Fig. 1 Function of the 8 x 8 bit SPPS-LSI

principle, the process steps of a 4-channel by 4-bit data example are shown in Fig. 3. It corresponds to a 4 x 4 shift register array. The conversion steps are as follows:

Step 1 - Step 4 : The preliminary data (A1,B1,C1,D1) are stored in the left-hand column. Next, the subsequent data (A2,B2,C2,D2) are stored, with the 1st data simultaneously shifted horizontally. In the same way, the subsequent data (A3,B3,C3,D3) (A4,B4,C4,D4) are stored and shifted one after another. At the end of step 4, the 4 x 4 array is filled.

Step 5 - Step 8 : Shift operation is changed from a horizontal to vertical direction. Fifth step data (A1',B1',C1',D1') are stored in the bottom row, and the top row data (A1,A2,A3,A4) are pushed out. Subsequent steps follow the previous pattern.

Step 9 : Shift operation is changed again from the vertical to horizontal direction, with 9th step data (A1'',B1'',C1'',D1'') stored in the left-hand column and right-hand column data (A1',A2',A3',A4') pushed out. Consequently, 4-channel by 4-bit data conversion is per-

formed by a cyclical operation from step 1 to step 8 like pipeline operation.

3. Circuit configuration

For an 8-channel by 8-bit case, the LSI block diagram is shown in Fig. 4. It consists of an (8 x 8) array of shift registers with 2:1 selectors, 8-bit output registers, a Row/Column timing control circuit, and I/O buffer gates. R/C is the transmission direction control signal. DR and DC are the data signals in the row and column directions. The array's high regularity effectively achieves small chip size and short design time. The maximum operating speed of this LSI is determined by the propagation delay of a shift register with a 2:1 selector.

In addition to the novel conversion method, a sophisticated circuit technique is adopted for the basic shift register circuit. A schematic of this circuit is shown in Fig. 5. In comparison with simple gate or 2-level series-gating construction, the number of elements and gate stages has been reduced by using a 3-level LCML series-gated structure. The internal logic swing is designed to be 450 mV with a differential driving to obtain high-speed operation. The power supply voltage is -3.5 V, and the switching current is 0.6 mA. By using the 3-level LCML series-gated structure and low logic swing, small cell size (196.5 x 159 μm), and low-power dissipation (4.2 mW/cell) are achieved.

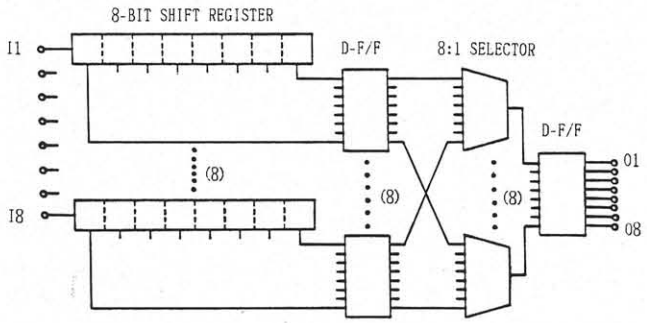

Fig. 2 Block diagram of the conventional 8 x 8 bit SPPS-LSI

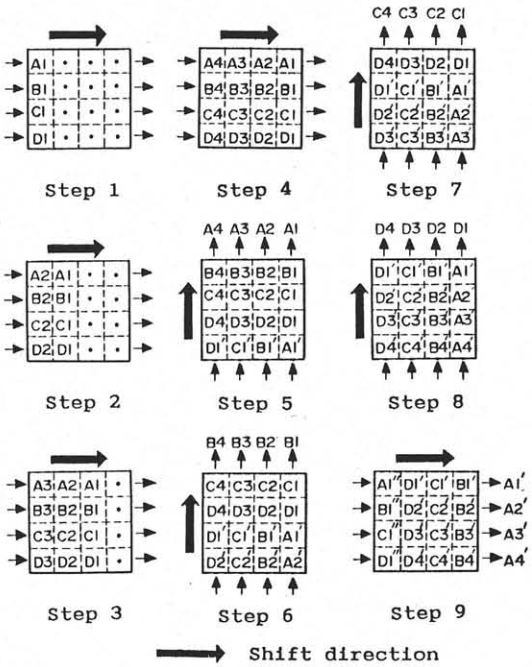

Fig. 3 Operating process of the novel SPPS conversion method

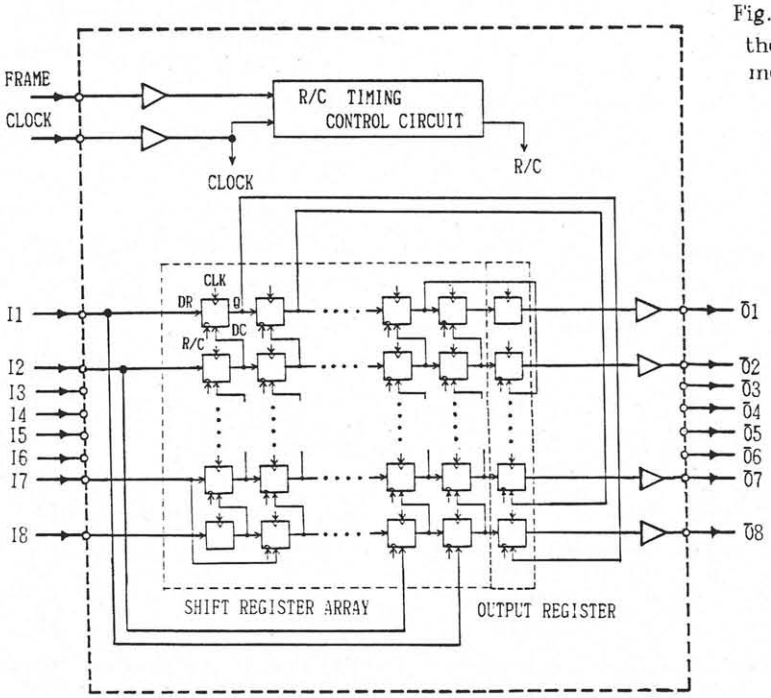

Fig. 4 Block diagram of the novel 8 x 8 bit SPPS-LSI

4. Fabrication

The SPPS-LSI is fabricated using a 1.0 μm rule Super Self-aligned process Technology (SST-1A). SST can realize the transistor active region without allowing a mask alignment margin. It is characterized by low base-collector junction capacitance, low base resistance, and high cut-off frequency [2]. The emitter size used is 0.5 x 8 μm. The basic transistor parameters used is 0.5 x 5 μm. The basic transistor parameters used are summarized in Table I. Two-level metallization is used. The wiring pitches of the first and second metal layers are 4 μm and 6 μm, respectively. A fabricated chip microphotograph is shown in Fig. 6. The size of the array is only 1.27 x 1.57 mm. The resulting total chip size is 2.5 x 3.1 mm. The components total 2093 (transistors: 1497, resistors: 596). The equivalent gate count is about 0.8K gates. The I/O interface level is ECL10K compatible with a 50 ohm termination. The main features of the fabricated 8 x 8 bit SPPS-LSI are summarized in Table II.

Table I Transistor characteristics

Emitter size	0.5 x 5 μm
Base series resistance	285 ohm
Base-emitter junction capacitance	8.2 fF
Base-collector junction capacitance	10.2 fF
Collector-isolation capacitance	41.2 fF
Cut-off frequency	12.4 GHz

Table II Main features of the 8 x 8 bit SPPS-LSI

Number of I/O	8-Input data 8-Output data Frame clock Main clock
Operating speed	1.56 GHz maximum
Power supply	1.09 W
Number of components	1497 transistors 596 resistors
Complexity	Equivalent 0.8K-gate
Chip size	2.5 x 3.1 mm
I/O interface	ECL10K
Process	1 μm SST-1A

5. Performance

A high-speed test was performed for the mounted chip into a high-speed flat package at room temperature. The measurement system was constructed of a 2.0 Gb/s pulse pattern generator, a sampling oscillo-

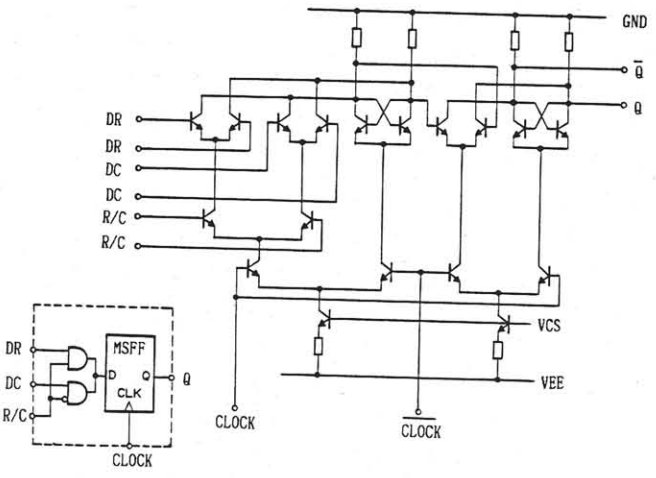

Fig. 5 Basic shift register circuit with a 2:1 selector using a 3-level series-gated technique

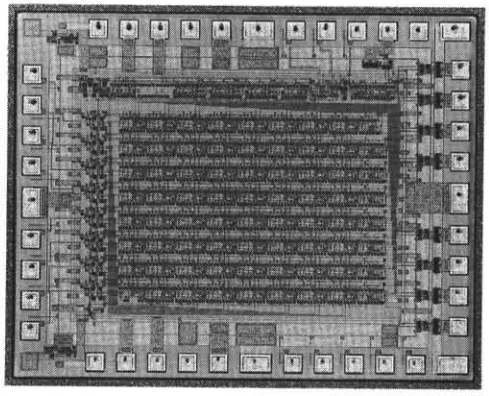

Fig. 6 Chip microphotograph. Chip size is 2.5 x 3.1 mm.

Input channel	Input data stream →
1	0 0 1 0 . . . 0
2	0 0 1 0 . . . .
3	0 0 1 0 . . . .
4	0 0 0 0 . . . .
5	0 0 1 0 . . . .
6	0 0 0 0 . . . .
7	0 0 0 0 . . . .
8	0 0 0 0 . . . 0

Output

(a) Test for a certain channel output.

Input channel	Input data stream →
1	0 0 0 0 . . . 0
2	1 1 1 1 . . . 1
3	0 0 0 0 . . . 0
4	1 1 1 1 . . . 1
5	0 0 0 0 . . . 0
6	1 1 1 1 . . . 1
7	0 0 0 0 . . . 0
8	1 1 1 1 . . . 1

Output

(b) Test for parallel 8 channel outputs.

Fig. 7 Input test patterns.

scope, and a high-speed logic analyzer (DAS-9100). As shown in Fig. 7, two kinds of input test data patterns (a) and (b) were used. A waveform example at 900 MHz for test pattern (a) is shown in Fig. 8. The upper trace is the 900 MHz clock signal and the lower trace is the converted serial output data pattern. Fig. 9 shows the parallel 8 outputs pattern for test pattern(b), measured by using the logic analyzer at 630 MHz. Because the minimum resolution time is limited to 500 ps, there are some variations in the timing edges. However, good operation is confirmed for all channels. Fig. 10 shows the data input sensibility characteristic for test pattern(a). A maximum operating rate of 1.56 GHz was achieved. Measured chip power dissipation is 1.09 W, which agrees well with the desined value.

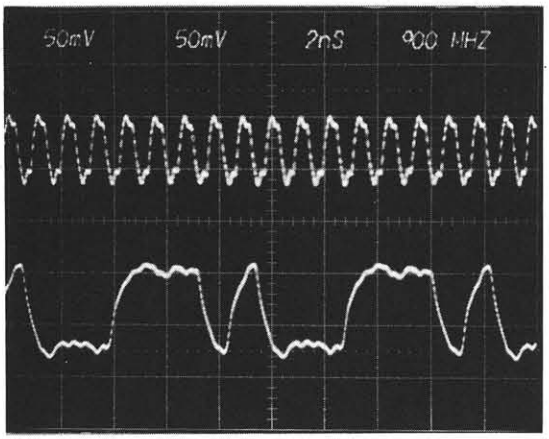

Fig. 8 Output waveform example at 900 MHz. Applied input test data pattern is (a).

6. Summary

An 8 x 8 Serial/Parallel, Parallel/Serial conversion LSI (SPPS-LSI) with 1.56 Gb/s throughput and 1.09 W/chip power dissipation has been developed using a novel conversion method, sophisticated circuit technique, and a Super Self-aligned process Technology (SST-1A). The technologies proposed here are very effective for achieving high-speed pipeline logic LSIs. Moreover, when the internal logic swing is reduced from 450 mV to 225 mV, even greater performance will be realized.

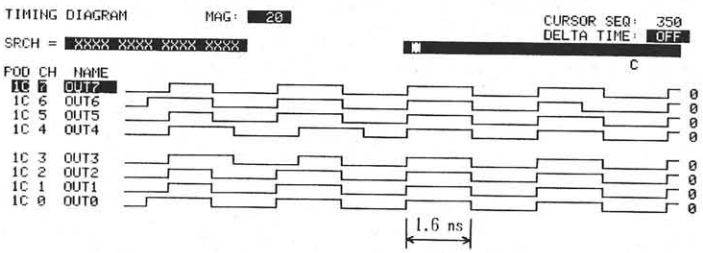

Fig. 9 Parallel 8 channel outputs by the logic analyzer. Applied input test data pattern is (b).

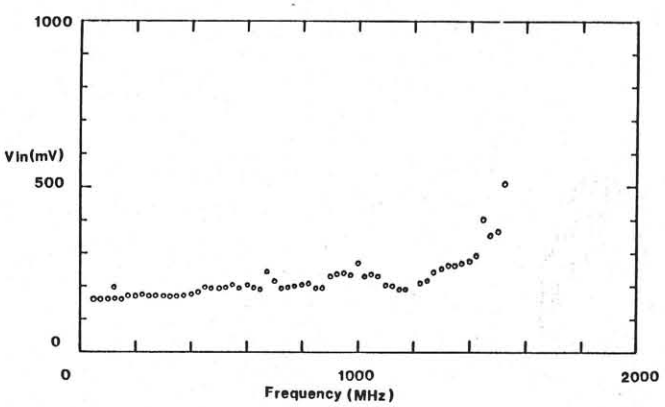

Fig. 10 Data input sensibility characteristic.

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