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Invited

Ultra High Speed Bipolar Device-SICOS

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Symmetrical npn transistors with a sidewall base contact structure(SICOS) are developed and high cutoff frequencies of 14 GHz in downward and 4 GHz in upward operation were obtained. Using these transistors, high speed ECL circuits, frequency divider circuits and multiplier circuits are constructed and their exellent performances are nearly equal to that of GaAs devices.

I. INTRODUCTION

It is well known that conventional device structures contain large parasitic capacitance areas that affect high speed operation. The delay time of ECL circuits constructed by conventional structures is about 200 ps, and it is difficuit to obtain a gate delay below 100 ps. On the other hand, the delay time limitation for IIL circuits has been considered to be about one nanosecond[1].

It is also known that reduction of parasitic elements dramatically improve the gate delay and packing density[4]. In order to accomplish the reduction of device size and the accompanying parasitic components, a newly self-aligned device structure must be utilized[2-10]. The symmetrical structure of a bipolar transistor is suitable for reducing device parasitic capacitances, and sidewall base contact structure, SICOS transistor[2, 8], is one of the most promising candidates for an ideal transistor.

In this presentation, recent advances in high speed bipolar device technology will be described and characteristics of SICOS transistors will be reviwed.

II. DEVICE STRUCTURE AND PERFORMANCE

A. CONVENTIONAL DEVICE

A conventional bipolar transistor structure, illustrated in Fig. 1, contains extrinsic base regions, which are over a magnitude larger than the intrinsic base regions. These regions are only necessary for base contact, and behave as parasitic capacitances in downward operation and as parasitic diodes in upward operation. These parasitic effects have increased the power dissipation and the delay time of gates. The extrinsic base regions should be excluded in order to improve performance.

B. POLYSILICON BASE SELF-ALIGNMENT TRANSISTOR

In order to eliminate parasitic regions, polysilicon self-alignment technology has been developed. In SST(Super Self-aligned process Technology) transistors[5, 11], illustrated in Fig 2, one photomask is needed to fabricate the emitter and base regions, including the submicron width base electrode and base and emitter contacts. Intrinsic base regions are constructed in single crystal substrate and polysilicon base electrodes are used to eliminate base series resistance and base-collector parasitic capacitances. An NTL circuit gate delay of 30 ps/G[12] and a 1kb ECL RAM with typical address access time of 0.85 ns[13] were obtained using this device.

Poly-base transistors with U-grooved isolation have been developed[14, 15]. Using

these, a minimum ECL circuit gate delay of 73 ps/G[16], and a 16 kb ECL RAM with an access time of 4 ns[15] were obtained. Further reduction of base resistance was accomplished by covering the polysilicon base regions with platinum silicide. 18 kG masterslice LSIs have been developed and intrinsic gate delay of 150 ps was obtained by 1.5 um rule SCOT[17].

C. SIDEWALL BASE CONTACT STRUCTURE(SICOS)

A sidewall base contact structure, illustrated in Fig. 3, utilizes polysilicon base electrode on buried silicon dioxide to minimize parasitic effects. Intrinsic regions of devices are formed in a mesa-etched substrate and connected to the polysilicon electrodes at the sidewalls. In the SICOS transistor, isolation, base contact, intrinsic base region, emitter region, and emitter contact are defined by only one photomask. This self-alignment technology enables a npn transistor to reduce the n-type buried layer regions and transistor cell size. Moreover, the symmetrical device structure provides high speed characteristics not only in downward but also in upward operations.

Figure 4 shows cutoff frequency as a function of collector current for SICOS NPN transistors. The emitter area is 2 um x 3 um, and an epitaxial layer of 0.7 um was adopted. Maximum cutoff frequency is 14 GHz for downward operated transistors, and 4 GHz for upward operated transistors[18, 19]. In conventional device structures, downward cutoff frequency is about 100 times larger than upward ones. SICOS transistors demonstrate a very high upward cutoff frequency, one that is slightly lower than the downward cutoff frequency. Table 1 summarizes the characteristics of SICOS NPN transistors.

Figure 5 shows measured IIL and ECL gate delay on the same chip as a function of power dissipation. These results were measured for a fanin or fanout of 1. The emitter dimensions are 2 um x 3 um. Minimum gate delay of 84 ps/gate[19] was measured for ECL at a collector current of 0.9 mA, while it is 96 ps/gate at a fanin of 3. For the IIL circuits, minimum gate delay was 320 ps/gate at a power dissipation of 5 mW/gate.

High speed ECL circuits were applied to frequency divider circuits[20] and multiplier circuits. Frequency divider contains 4 stage divide-by-two circuits with 3 internal buffers and output buffers. The current level of each transistor flows as 1 mA. The relation between input power and dividing frequency is shown in Fig. 6. A maximum dividing toggle frequency of 6.9 GHz can be attained at a power/stage of 45 mW.

IIL frequency divider circuits are also fabricated. The maximum dividing frequency of 580 MHz was obtained at a power/stage of 9 mW. The characteristics of the frequency divider circuits are summarized in Table 2. A 1/64 frequency divider was constructed by mixing ECL and IIL flip-flops, and could be optimized to operate above 6 GHz with total power consumption of less than 100 mW.

An 8 x 8 bit parallel multiplier, whose architecture was constructed with carry save adder(CSA) arrays and CLA, was fabricated using 2 um x 3 um SICOS transistors. Results are also shown in Table 2. A multiplication time of 2.7 ns was obtained at a power dissipation of 900 mW.

III. HIGH SPEED BIPOLAR LSI AND GaAs LSI

GaAs FETs are considered to be the most promising candidate for LSIs used with a gate delay below 100 ps. Since the fabrication of self-aligned silicon bipolar transistors, their high speed performance has become nearly equal to that of GaAs devices. The performance of silicon and GaAs devices are compared at the circuit level. Maximum dividing frequency and power dissipations of these devices are shown in Fig. 7. The silicon ECL frequency divider has features of high power dissipation and middle frequency speed. Meanwhile, GaAs frequency divider circuits have features of low power dissipation and higher frequency speed. The SICOS ECL and IIL frequency divider has low power and high speed performance which is close to that of GaAs devices.

The characteristics of multiplier circuits are also compared in Fig. 8. Multiplication time delay per bit was taken into account to compare the circuits with different configuration. Silicon bipolar devices have the possibility of constructing higher speed circuits than GaAs devices by comsuming more power.

IV. CONCLUSION

Recent advances in bipolar devices have been described. Self-aligned bipolar transistors have excellent high speed characteristics. In particular, SICOS transistors provide high speed and low power performances close to those of the GaAs devices.

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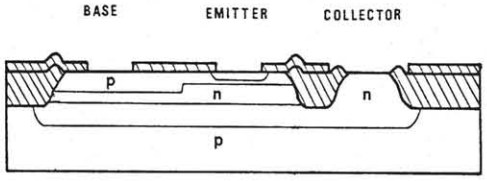

Fig. 1. Conventional npn transistor structure.

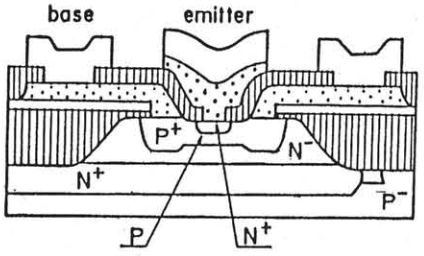

Fig. 2. SST transistor structure.

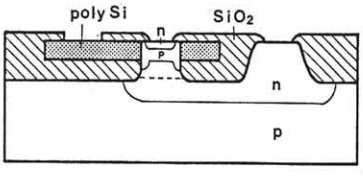

Fig. 3. SICOS transistor structure.

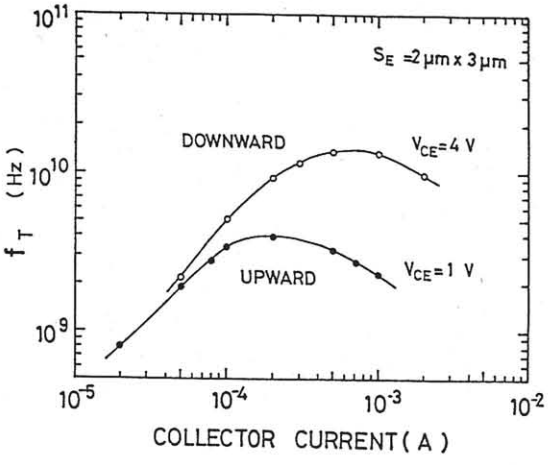

Fig. 4. Cutoff frequency characteristics of SICOS transistor.

Table 1.

CHARACTERISTICS OF SICOS NPN TRANSISTOR	
CELL AREA	128 μm^2 (S_E= 2μm X 3μm)
h_{FE} (downward)	50 (Ic=100μA)
h_{FE} (upward)	70 (Ic=100μA)
C_{CB}	8 fF
C_{EB}	18 fF
C_{CS}	15 fF
rbb'	500 ohm (Ic=0.5mA)
f_T (downward)	14 GHz
f_T (upward)	4 GHz

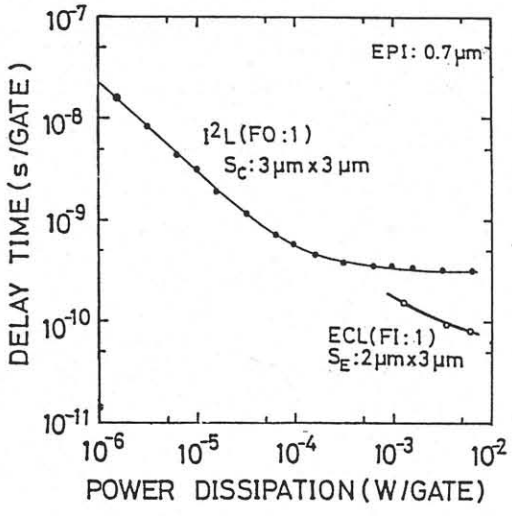

Fig. 5. Relation between delay time and power dissipation of ECL and IIL circuits.

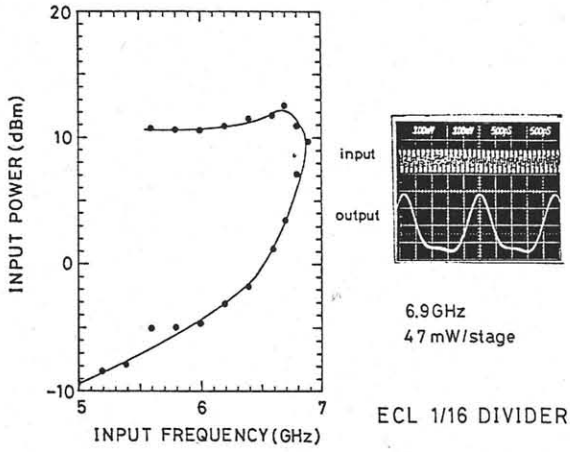

Fig. 6. Characteristics of frequency divider circuits.

Table 2.

CHARACTERISTICS OF FREQUENCY DIVIDER AND MULTIPLIER CIRCUITS

FREQUENCY DIVIDER	finmax	6.9 GHz
	POWER	45 mW
	V_A	400 mV
MULTIPLIER	BIT SIZE	8 X 8
	MULTIPLICATION TIME	2.7 ns
	POWER DISSIPATION	900 mV(4.5V)
	CHIP SIZE	1.7 X 2.0 mm²

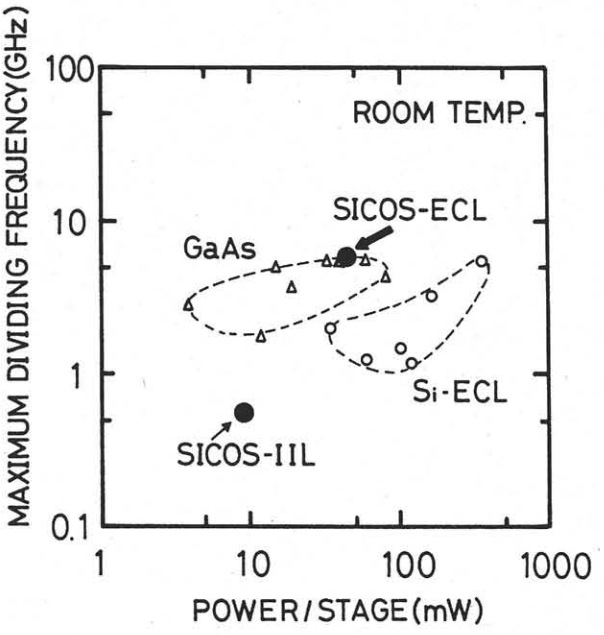

Fig. 7. Comparison between dividing frequency vs. power of silicon bipolar and GaAs circuits.

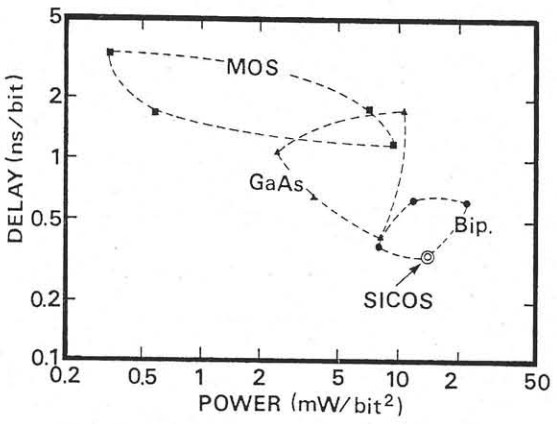

Fig. 8. Comparison of multiplier characteristics between silicon and GaAs devices. The plotted points represent multiplier reported elsewhere.