

Compact Bipolar Transistor Model for CACD, with Accurate Description of Collector Behaviour

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Abstract

A new compact bipolar transistor model, called MEXTRAM, for CACD purposes is presented. It is not based on the charge control principle, but it describes the main currents and charges separately in terms of bias dependent minority carrier concentrations.

Two features are stressed: a refined modeling of the collector epilayer phenomena, including hot carrier effects, and the influence on the high-frequency behaviour of splitting base and collector resistances and collector capacitance.

1 Introduction

In principle there are two ways of modeling the behaviour of electron devices:

- computer simulation by solving numerically the transport equations with appropriate boundary conditions
- by finding a compact set of analytical equations.

The last method is sometimes less accurate, but has the great advantage of a fast numerical evaluation and is therefore used in circuit simulators like SPICE and PHILPAC. For bipolar transistors there exist already such compact models like the Ebers-Moll (E-M) model and the Gummel-Poon (G-P) model [1,2]. Both make use of the charge control principle, which says that a stored charge Q is linearly proportional to its related current I ($Q = \tau \cdot I$). The proportionality factor is the carrier transit time.

Recently a set of compact model equations for the bipolar transistor was published [3], that does not rely on charge control relations. The main currents and charges were formulated in that publication, but a complete transistor model description was not given. We will make up for this omission by putting forward two other features:

- an extensive modeling of the phenomena in the collector epilayer, including hot carrier effects,
- the splitting up of the collector capacitance and base and collector series resistances.

In this way we developed a complete compact bipolar transistor model for circuit simulation called MEXTRAM, that is in many respects superior to the E-M and G-P models, especially in the high current ranges of the F_i and h_{FE} fall-off. In the next sections the major components of the MEXTRAM model will be discussed and typical examples will be given, also in comparison to the E-M and G-P models.

2 Main currents and charges

The equivalent scheme of the model is given in fig. 1. I_f and I_r are the forward and reverse currents, Q_{be} and Q_{bc} the stored charges in the base. $I_f(n_0)$ and $Q_{be}(n_0)$ are different functions of the minority carrier concentration n_0 in the base, injected from the emitter [3]. By making use of the p - n product for junctions and assuming charge neutrality, this n_0 in turn, becomes a function of the internal V_{b2e1} :

$$(n_0 + N_A)n_0 = n_i^2 \exp\left(\frac{qV_{be}}{kT}\right) \quad (1)$$

In this way high injection is automatically incorporated.

I_r and Q_{bc} are treated similarly: they are functions of n_b , which does not depend directly on V_{c2b2} , but is coupled to the injected minority carrier concentration p_0 in the collector epilayer:

$$(n_b + N_A)n_b = (p_0 + N_{epi})p_0 \quad (2)$$

where p_0 depends on V_{c2b2} .

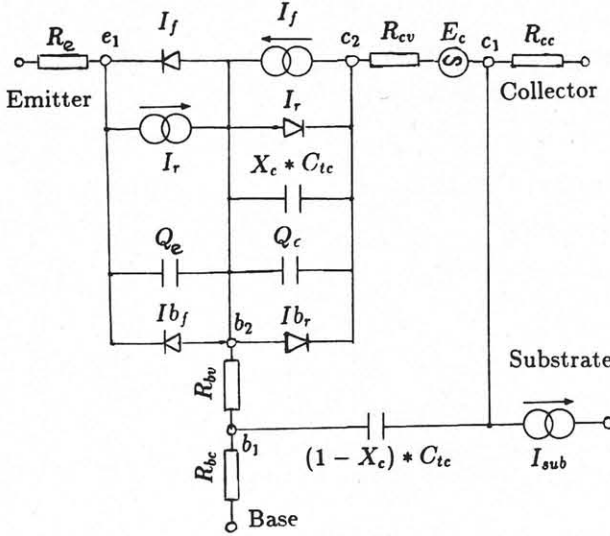


fig. 1 Equivalent circuit diagram for MEXTRAM

Forward and reverse base transit times, defined as:

$$\tau_f = \frac{dQ_{be}}{dI_f} \quad \text{and} \quad \tau_r = \frac{dQ_{bc}}{dI_r}$$

are now automatically bias dependent.

A bias dependent Early effect is introduced by the factor:

$$\left\{ 1 + \frac{Q_{Te} + Q_{Tc}}{Q_{b0}} \right\} \quad (3)$$

where Q_{Te} and Q_{Tc} are the depletion charges at the emitter and collector sides respectively and Q_{b0} is the equilibrium base charge. On Q_e in fig. 1 are assembled the charges Q_{be} , Q_{Te} and the charge storage in the emitter Q_n .

Base current components are added and the base resistance is split into a constant part R_{bc} outside the emitter and a bias dependent part R_{bv} under the emitter.

3 Collector charging times

In MEXTRAM the total collector depletion capacitance C_{Tc} is split into an active transistor part $x_c \cdot C_{Tc}$ under the emitter and the remainder $(1 - x_c) \cdot C_{Tc}$ in the inactive region. C_{Tc} depends on the internal voltage V_{c2b2} and is modeled as given in [4]. The total collector series resistance consists of a fixed part R_{cc} in the buried layer and a variable part dV_{c1c2}/dI_c , which for low currents equals the epilayer resistance R_{cv} . The collector charging time is given by:

$$\tau_c = (R_e + R_{cc} + \frac{kT}{qI_c})C_{Tc} + \frac{dV_{c1c2}}{dI_c}x_cC_{Tc} \quad (4)$$

Especially at high current levels and hot carrier behaviour in the epilayer, dV_{c1c2}/dI_c becomes large and

for shallow junctions ($< 0.25\mu\text{m}$) τ_c may then equal the emitter and base transit times.

In a typical shallow junction process we have e.g. $\tau_e = 18$ ps., $\tau_b = 2$ ps. and $\tau_c = 10$ ps. at the top of F_t .

4 Modeling the collector epilayer

In MEXTRAM the collector epilayer description is an intrinsic part of the model and not treated as an extra modular unit [5]. The internal collector base voltage (V_{c2b2} in fig. 1) is determined by the externally applied voltage V_{cb} and the collector current I_c :

$$V_{c2b2} = V_{cb} - I_c \left(R_{cc} + \frac{dV_{c1c2}}{dI_c} - \frac{R_{bv} + R_{bc}}{h_{FE}} \right) \quad (5)$$

Below the critical current for hot carrier behaviour $I_{hc} = q \cdot N_{epi} \cdot v_{lim} \cdot A_{em}$, the voltage source E_c is a function of V_{c1b2} , in such a way that $E_c = -V_{DC}$ (diffusion voltage) for reverse biased junctions and at forward bias (fig. 2a):

$$E_c \approx 2 \frac{kT}{q} \exp \left\{ q(V_{c1b2} + V_{DC})/kT \right\} \quad (6)$$

An internally forward biased collector ($V_{c2b2} < 0$) also gives rise to injection into the collector epilayer with a charge storage Q_{epi} . We then have [4]:

$$Q_{epi} = q \int_{epi} p_0 dx \quad (7)$$

and

$$2p_0 + \ln p_0 = \frac{q}{kT} V_{c2b2} \quad (8)$$

For $I_c > I_{hc}$ we will have hot carriers in the epilayer, which will cause an extra voltage drop, modeled as an increase ΔE_c in the voltage source E_c (see fig. 1). This ΔE_c is a complicated function of V_{c1b2} and I_c and is shown in fig. 2b. The decrease of ΔE_c at very high current levels corresponds with an increasing saturation and shrinking space charge region in the epilayer.

5 Some examples

The first example is a BIMOS bipolar npn transistor [6]. The epilayer thickness between buried layer and base is about $2\mu\text{m}$, with $N_{epi} \approx 5 \cdot 10^{15}\text{cm}^{-3}$. Fig. 3 gives $F_t(I_c, V_{cb})$ for a $7 \times 9\mu\text{m}$ emitter transistor. At the maximum F_t the collector contribution is 10 ps to a total delay of 50 ps, at 3 mA it is already 30 ps out of 75 ps. So the collector delay and RC-times are very important here and the correct modeling of F_t fall-off cannot be obtained with a simple collector representation as in the G-P model (fig. 3b).

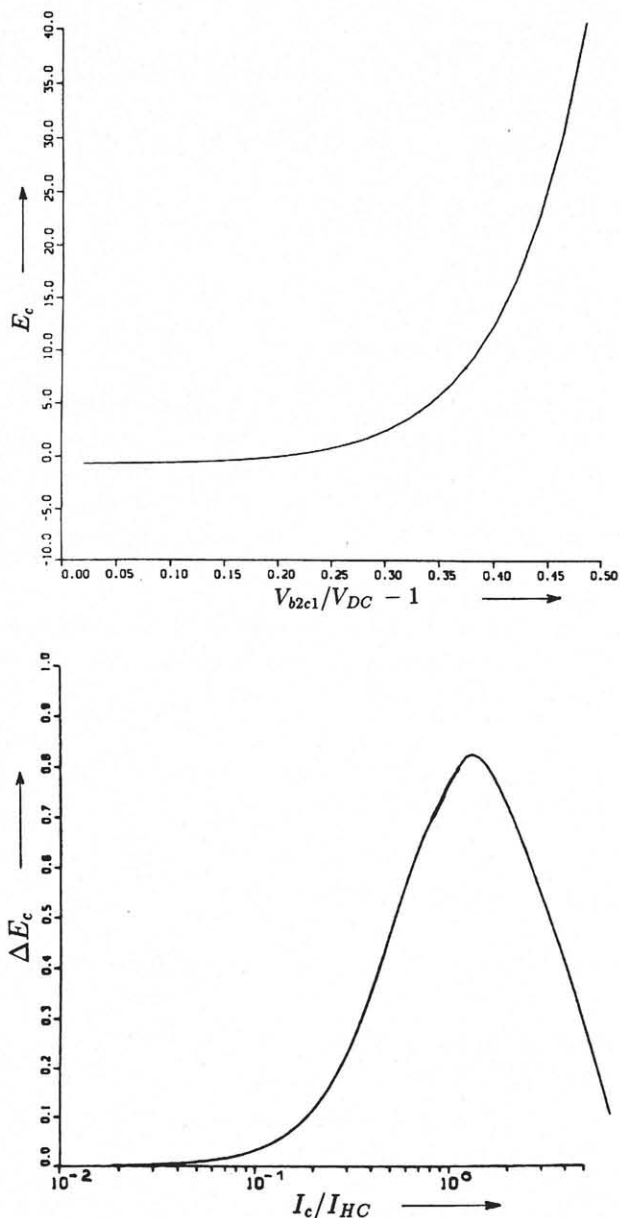


fig. 2. a) The voltage source E_c as a function of the applied voltage V_{c1b2} . b) The extra hot carrier voltage drop ΔE_c as a function of the normalized collector current.

Refined modeling of the saturation also gives a better fit of the $I_c(V_{ce})$ characteristics at low collector voltages (knee behaviour), see fig. 4.

Another example is that of a microwave transistor with 14 emitter stripes ($18 \times 0.75 \mu\text{m}^2$), an epilayer thickness of $1.2 \mu\text{m}$ and an epilayer dope $N_{epi} = 3 \times 10^{15} \text{cm}^{-3}$. The $I_{hc} = 35 \text{ mA}$ in this case, causing a hot carrier voltage drop in the epilayer, which means that a large part of the useful $I_c(V_{ce})$ characteristics is governed by

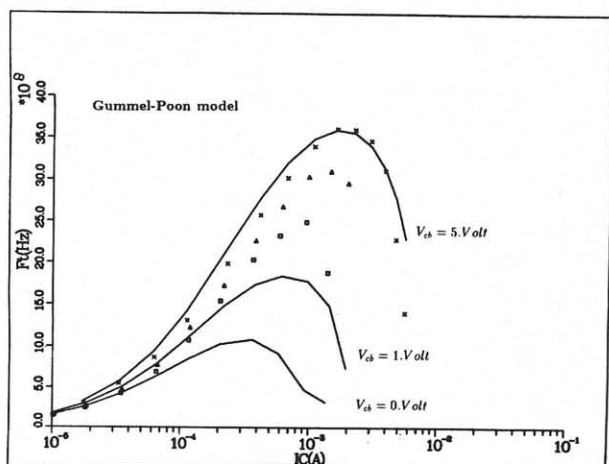
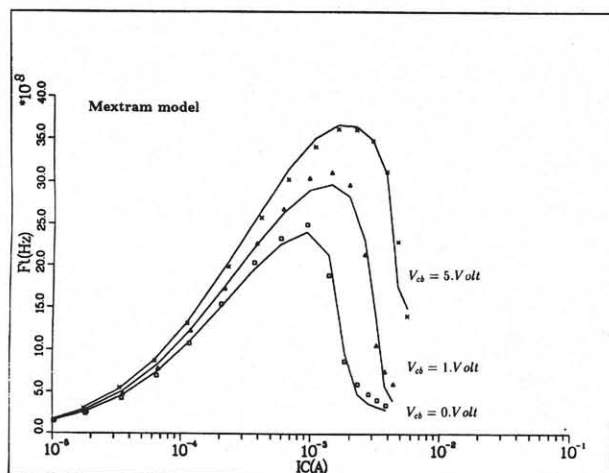


fig. 3. a) The cut-off frequency F_t vs. I_c for different V_{cb} values. Fully drawn lines are model calculations with MEXTRAM, measured values are indicated by \square , \triangle and \times . b) As in fig. 3a, but now for the G-P model.

quasi-saturation. Nevertheless MEXTRAM can model this quite adequately, as shown in fig. 5.

To show the possibilities of the new model in a complete circuit simulation we give the example of a ring-oscillator with 11 ECL OR-gates and 1 NOR gate. The measurements revealed an oscillating frequency of 84.7 MHz. We have done circuit simulations with MEXTRAM, G-P and E-M models. The results are given in table 1. The transistors are used at their maximum F_t , so quasi-saturation is not important here. The $r_b \cdot C_{tc}$ product however is, and so is the bias dependence of C_{Tc} and the splitting up of base and collector resistances. Table 1 also gives the CPU-times for a transient run. The simplest model is also the fastest.

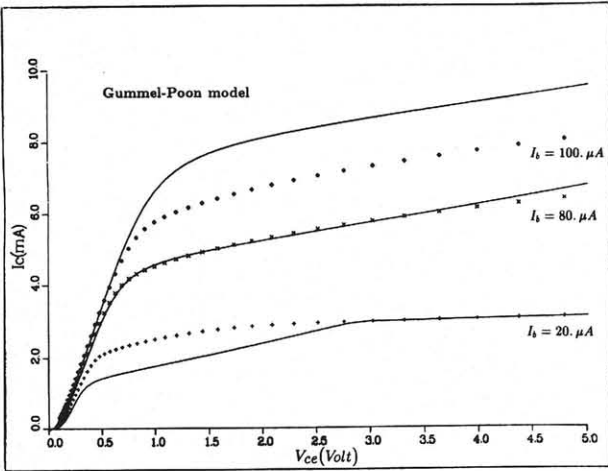
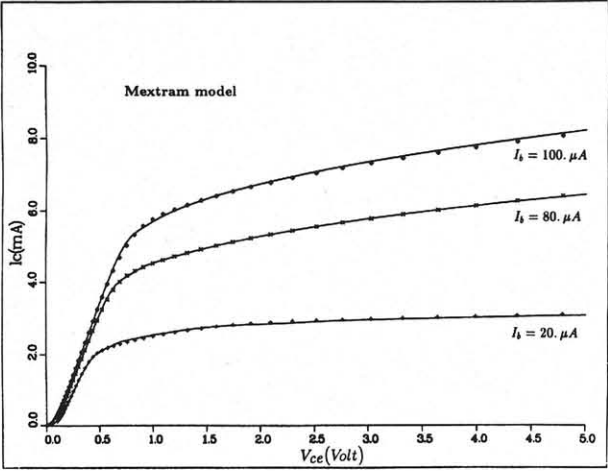


fig. 4. $I_C(V_{CE})$ characteristics of the BIMOS transistor as in fig. 3.

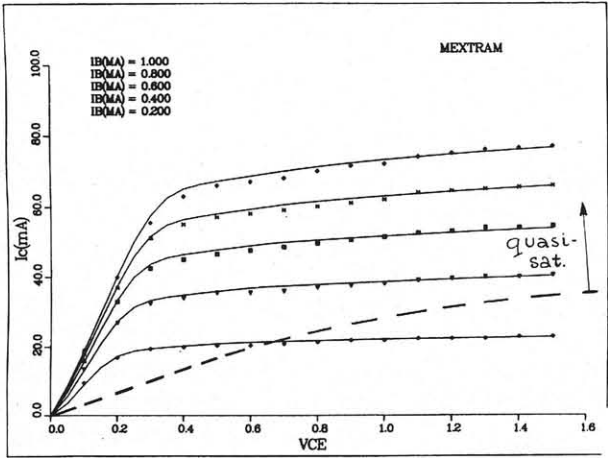


fig. 5 $I_C(V_{CE})$ characteristics of a microwave transistor with $W_{epi} = 1.2\mu m$ and $N_{epi} = 3 \times 10^{15} cm^{-3}$.

Table 1

	frequency	CPU-time (rel.)
measurement	84.7 MHz	-
Ebers-Moll	56.5 MHz	1.
Gummel-Poon	92.5 MHz	1.5
Mextram model	84.4 MHz	3

6 Conclusions

A new compact bipolar transistor model is presented. Apart from a reformulation of the main currents and charges, much attention has been paid to the correct modeling of C_{Tc} and the split up of that C_{Tc} and series resistances r_b and r_c . Moreover, the model incorporates a better epilayer behaviour description, including hot carrier behaviour.

All this results in an improved prediction of F_t fall-off, of the $I_C(V_{CE})$ characteristics at low V_{CE} and in more accurate circuit simulation results.

References

- [1] J.J. Ebers and J.L. Moll, Proc. I.R.E. 42, 1761 (1954)
- [2] H.K. Gummel and H.C. Poon, Bell Syst. Techn. J. 49, 827 (1970)
- [3] H.C. de Graaff and W.J. Kloosterman, IEEE Trans. Electr. Dev. ED-32, 2415 (1985)
- [4] H.C. de Graaff, in Process and Device Modeling for Integrated Circuit Design, ed. v.d. Wiele, Engl and Jespers, Noordhoff-Leiden (1977).
- [5] G.M. Kull, L.W. Nagel, S.W. Lee, E.J. Prendergast, P. Lloyd and H.K. Dirks, IEEE Trans. Electr. Dev. ED-32, 1103 (1985).
- [6] F. Rausch, H. Lindeman, W. Josquin, D. de Lang and P. Jochems, An analog BIMOS technology, this digest.