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Peripheral Capacitor Cell with Fully Recessed Isolation for Megabit DRAM

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Peripheral capacitor cell is presented. A side wall of a grooved isolation was utilized as a part of memory capacitor, and at the bottom of the groove a field oxide was selectively grown. Oblique implantation was used to form a Hi-C structure in a side wall. The cell capacitance was increased about 50% by grooving only 0.6 um, and cell to cell isolation could be reduced to 0.6 um.

INTRODUCTION

The major problem for realizing future high density DRAM is to maintain a cell capacitance sufficiently large, e.g. above 50 fF, in a very small cell size which has to satisfy chip size requirements. For this purpose the trench capacitor cell(1) was developed to fabricate 1M bit(2) and experimental 4M bit(3) DRAM's. However, the trench capacitor cell has inherent drawbacks of trench to trench isolation(4), and of alpha particle induced soft error. Folded Capacitor Cell (FCC)(5) and Buried Isolation Capacitor cell (BIC)(6) were proposed to overcome these drawbacks, where a relatively shallow trench was formed around the memory cell and was utilized as a storage capacitor as well as an isolation.

We developed the Peripheral Capacitor Cell (PCC) with fully recessed field oxidation technique, and also a double diffused Hi-C structure in a side wall by using oblique ion implantation. This process provided a better control of isolation characteristics and also a high immunity of soft error.

In this paper, we describe the PCC structure, the fabrication process, and experimental results on this new DRAM cell.

PCC MEMORY CELL STRUCTURE

The PCC cell structure is illustrated in Fig.1 in comparison with the trench capacitor cell. The basic concept of PCC is to utilize the relatively long periphery of a memory cell as an additional area for storage capacitance. The perimeter of a memory capacitor is 2-3 times longer than that of a trench capacitor in case of 1.2um design rule. This ratio increases when a feature size is further scaled down. Accordingly the grooved depth of PCC is much shallower than that of a trench capacitor. A wide opening and a shallow depth of the groove result in a better control of grooved shape and side wall doping, and also eliminate difficulties in cleaning deep and narrow trenches.

PCC can overcome isolation limitations of a trench capacitor cell imposed by punch-through current between adjacent trenches. In a PCC structure, a memory capacitor is effectively isolated from adjacent memory cells by a thick field oxide at the bottom of a groove.

It is quite difficult to construct a Hi-C structure(7) in a deep trench capacitor. In a PCC structure, a groove depth is much shallower, and then an oblique implantation can form heavily doped N+ and P layers at the side wall of the groove.

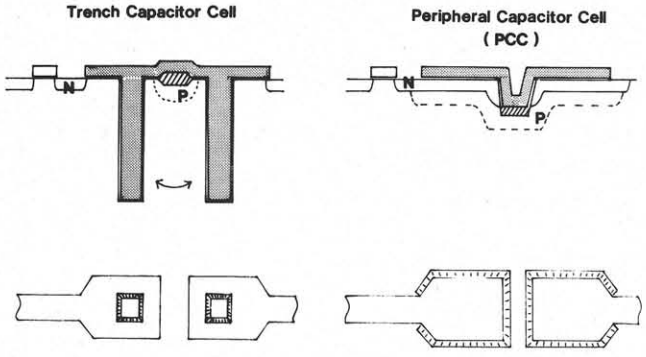

Fig.1 Schematic drawings of peripheral capacitor cell and trench capacitor cell

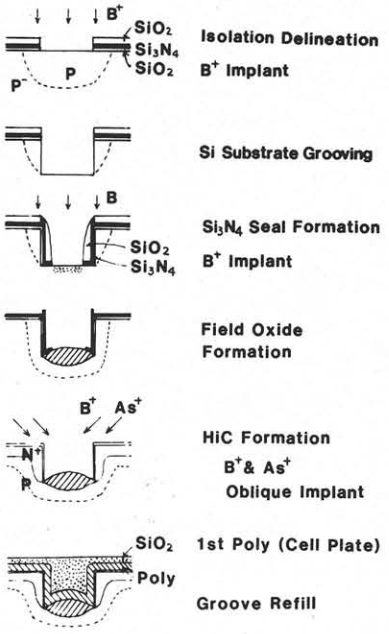

Fig.2 Fabrication process for PCC.

FABRICATION PROCESS FOR PCC

The main fabrication processings for PCC structure are shown in Fig.2. N-channel memory cells were fabricated in a P-type substrate. Isolation patterns were delineated in a composite layer of CVD oxide / nitride / pad oxide by using reactive ion etching. Boron was implanted into the isolation region and then diffused, in order to increase the boron concentration at the corner of the groove. The isolation region was then grooved anisotropically to a depth of 0.3-1.5um by reactive ion etching. Nitride and oxide films deposited with LPCVD covered the grooved surface conformally. The anisotropic etching of this composite layer resulted in a nitride seal at the side wall of the groove. The second boron implantation was done for channel stop at the bottom of the groove. A field oxide was selectively grown at the bottom to a thickness of 500 nm. Removal of the nitride seal completed the formation of the grooved isolation in a memory cell array.

The Hi-C structure was formed by using oblique implantation of boron and arsenic. The oblique implantation system developed can provide implant angle of 0 to 60 degree, which is adjusted according to the aspect ratio of the groove, and rotates the silicon wafer automatically. With this oblique implantation, and a photoresist as an implant mask, heavily doped N+ and P layers were formed at the horizontal surface and also the side wall of a memory capacitor.

10nm silicon dioxide was grown as a capacitor dielectric film, and the first poly-silicon layer was deposited to form cell plates. The grooves were then filled with CVD oxide and planarized by an etch back technique. Subsequently, gate oxide, polycide word lines, source/ drain, aluminum bit lines were formed to complete memory devices. Figure 3 shows a cross sectional SEM photograph of the PCC memory cell parallel to a word line.

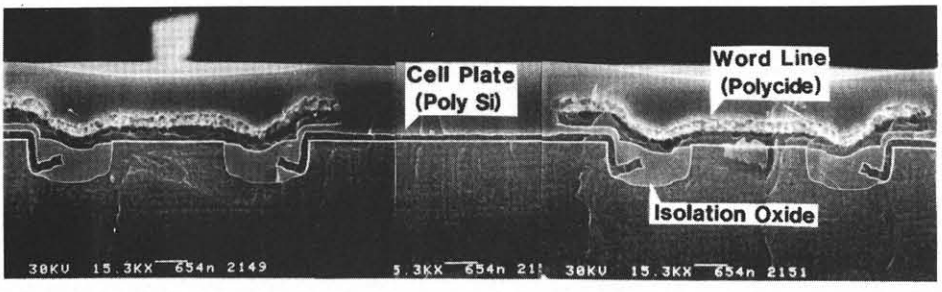

Fig.3 Cross sectional SEM photograph of PCC structure.

DEVICE CHARACTERISTICS

To ensure a large capacitance, it is necessary to form thin capacitor dielectric films together with heavily doped N+ layer in the side wall of grooves, in a Vss cell plate configuration. 10 nm silicon dioxide was grown as capacitor dielectric. The oxide at the side wall, however, became 20-30% thicker than the horizontal surface due to the crystal axis orientation. The dielectric integrity was improved by a sacrifice oxidation and a relatively higher oxidation temperature, and became comparable with the planar capacitor.

The heavily doped N+ layer, which was formed by oblique implantation of arsenic, could suppress depletion layer formation underneath the capacitor oxide. Figure 4 shows the efficiency of capacitance utility, which is defined as a ratio of the storage capacitance to the saturation capacitance in an accumulation mode, as a function of cell plate bias. The capacitance efficiency in a Vss cell plate was 84% in the PCC structure, compared with 87% in the planar capacitor.

The PCC structure with 10nm capacitor oxide and a heavily doped N+ layer resulted in an increase of cell capacitance to 60 fF with 0.6um groove depth, compared with 40 fF of the planar structure with 1.2um design rule, as is shown in Fig.5.

In a PCC structure, the field oxide was thermally grown and then its thickness could be precisely controlled. Channel stop boron implant could be increased without degrading narrow channel effects of a transistor. And there was no charge storage region deeper than an isolation region. With these advantages, PCC structure resulted in an excellent isolation characteristics. Figure 6 shows the cell to cell leakage current. Punch-through currents were not observed down to 0.6um cell to cell spacing. The breakdown voltage was 12.5V, which was determined by an avalanche breakdown between the capacitor N+ region and the channel stop P+ region.

A transistor in a memory cell array, such as transfer gate, would suffer from leakage current along the isolation, which is a major problem of a grooved isolation caused by a concentration of

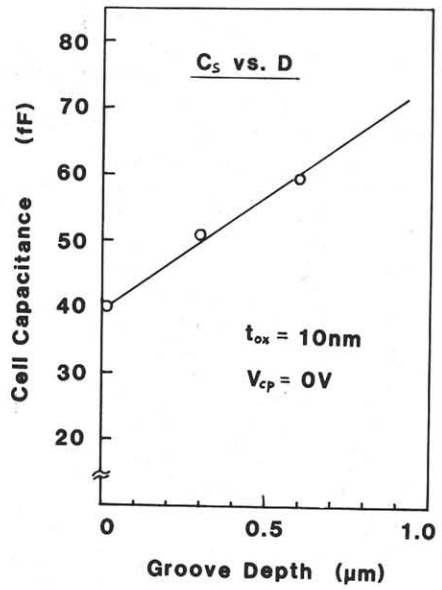

Fig.5 Storage capacitance vs. groove depth.

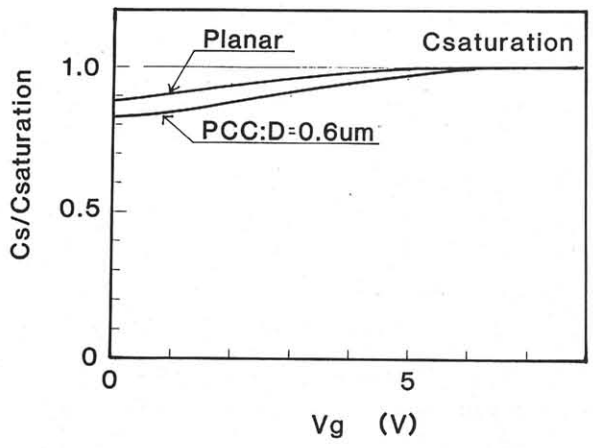

Fig.4 Efficiency of storage capacitance utility.

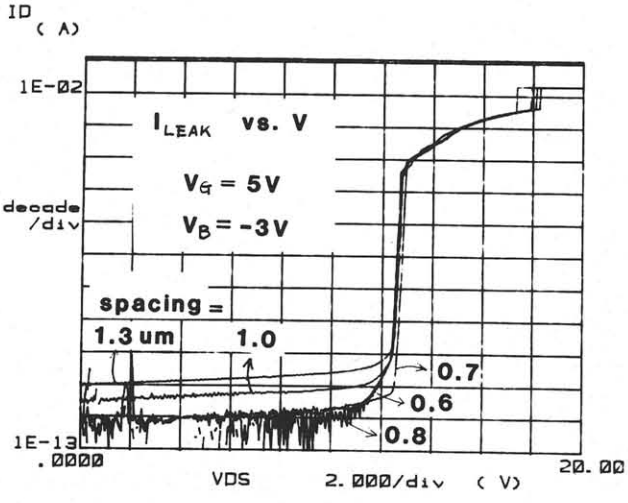

Fig.6 Cell to cell leakage current as a function of applied voltage.

electric field at the corner. A parasitic transistor action at the corner could be suppressed by filling the groove with CVD oxide, and by increasing the boron concentration at the corner. The boron doping was done prior to the isolation grooving, as is shown in Fig.2. Sub-threshold characteristics of a transfer gate are shown in Fig.7, and there were neither kinks nor humps.

256K and 1M bit DRAM were fabricated to examine a feasibility of PCC structure, and fully functional chips have been obtained. When a groove depth was 0.6 um and capacitor oxide was 10nm, the storage capacitance was measured to be 95 fF and 60 fF in 256K and 1M bit DRAM, respectively. The results on a pause refresh time measurements, shown in Fig.8, indicate that the leakage currents between adjacent cells and of transfer gates were extremely small. The soft error rates were also improved by a large storage capacitance, and also the funneling of the created carriers could be effectively suppressed by the Hi-C structure in a side wall capacitor.

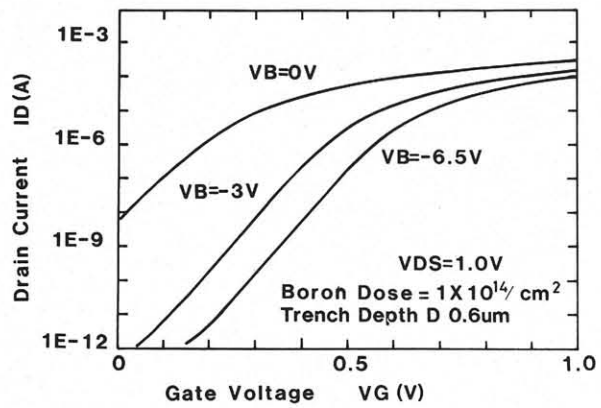

Fig.7 Sub-threshold characteristics of transfer gate transistor.

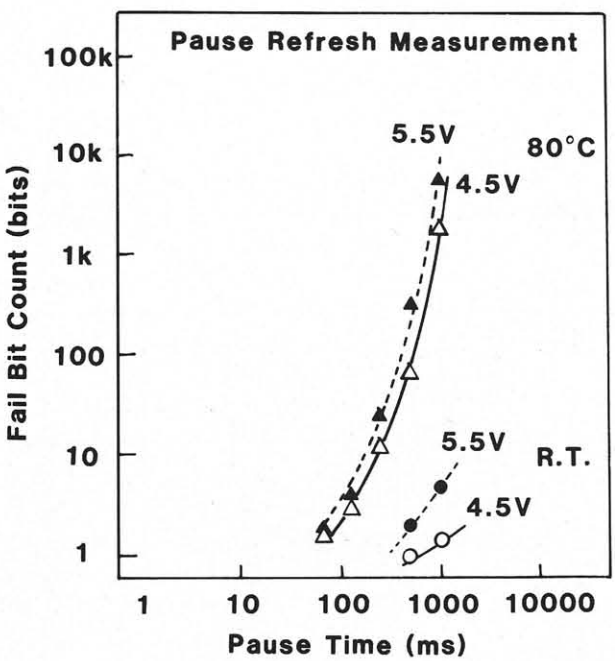

Fig.8 Pause refresh time characteristics of PCC.

CONCLUSIONS

The peripheral capacitor cell was proposed for future megabit DRAM's. In a 0.8 um design rule, the groove depth of 1.5 um and capacitor oxide of 10 nm will result in a stroge capacitance of 50 fF. Cell to cell isolation can be reduced to less than 0.6um with the isolation merged nature of this PCC structure. With a wide opening and a shallow groove, the oblique implantation can easily form a double diffused Hi-C structure at the side wall.

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