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Doping of Trench Capacitors for 4 Megabit DRAMs

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Trench capacitor doping via P-doped CVD-oxides (TEOS, LTO), As spin-on Glass, direct As-ion implantation and selective As Si-epitaxy is presented. Doping profiles, C(V) and trench to trench punch through data prove that only As doped trenches fulfill 4 Mbit requirements.

I. Introduction

Threedimensional structures like stacked or trench capacitors are required for sufficient storage capacitances of 4 Mbit DRAM cells (ref.1). To lower the electric field a mid-level-concept (e.g. + 2.5V on cell plate) is favoured (ref.2). A n^+ doping of the trench surface is then nessessary for threshold shift by several volts. The doping must be shallow to allow for trench to trench distances of 1-2 μm. In this paper trench doping via Phosphorous doped CVD oxides, Arsenic doped spin-on-glasses, direct Arsenic ion implantation and selective in-situ As doped epitaxial silicon growth is described. SEM cross sections, SIMS profiles, C(V) curves and gate oxide yields are discussed. Trench to trench punch through measurements show a strong dependence on junction depth and substrate doping concentration.

II. Doping techniques

Trenches were Phosphorous doped by depositting 300nm 4wt.% P LTO-oxide or 300nm 2.5wt% P TEOS-oxide. Phosphorous was driven in at 900-1000°C for 10-60 minutes in N_2. TEOS was used because of its better step coverage compared to LTO. Both oxides yield homogeneous doping profiles in the trench. After drive-in junction depth is 0.3 to 1.0 μm. Fig.1 shows greater depth for P TEOS than P LTO for the same drive-in.

A 0.9wt% As spin-on-glass (As SOG) was spun on at 3000 RPM for 10 seconds and solvents were evoporated by a 400°C bake resulting in a 170nm SiO_2 layer. During trench doping the planar surface was masked by nitride or oxide so only trenches were coated with As SOG. The As SOG thickness on the trench sidewalls is rather uniform but the thickness at the trench bottom depends on the trench shape. Drive-in ambient and temperature were varied. An ambient of N_2/O_2=9/1 gave the shallowest depth profiles. SIMS doping profiles for 1000°C and 950° are given in Fig.1. The profiles were less steep in pure N_2 and the As surface concentration was higher at 950°C than at 1000°C. To test the ion implantation technique As ions were implanted into deep trenches using a medium current implanter with a

mean beam tilt angle of 7 deg.
Dependence on tilt angle, screening oxide and drive-in conditions were studied with ion doses of 10^{15}-$10^{16}cm^{-2}$ and ion energies of 25-180keV. Considerable doping in the shadow region could be obtained only if no screening oxide was used and a thin oxide was grown prior to drive-in. Junction depths from SEM analysis were below 0.15 μm at the sidewalls and 0.30 μm at the bottom.
A strong dependence on trench shape was observed.

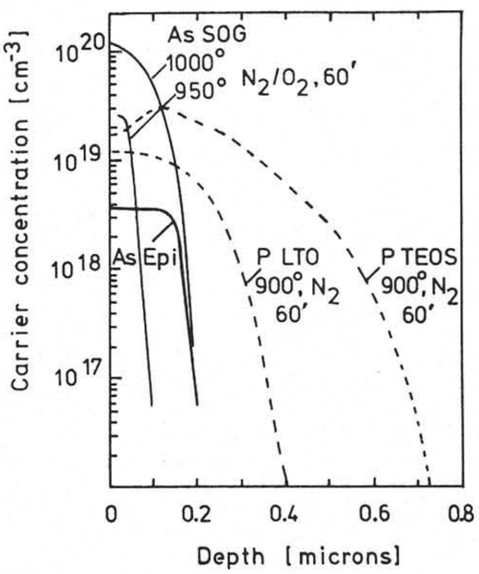

Fig.1: SIMS profiles for As SOG and As Epi techniques and spreading resistance measurements for P TEOS and P LTO

A new method for trench doping is the selective gas phase epitaxy of As doped silicon into the trenches. A cleaning process at 1050°C in H_2/HCl resulted in a rounded trench. The wafer surface was masked by pad oxide/nitride or TEOS-oxide and conformal selective epitaxial silicon was grown in the trench.
Epitaxial layers grown on planar surface at 950°C were 0.15 μm thick and had a steep As profile (Fig.1).
TEM cross sections of As-Epi in trenches showed no crystal defects at sidewall and bottom of trenches. Trenches with nitride layers on planar surfaces, however, showed twin-defects at the epi/nitrid interface, probably due to stress.

An example of As-Epi layer of 0.12 μm ($5x10^{18}cm^3$, As) in deep trenches of 0.7 μm diameter is shown in Fig. 2.

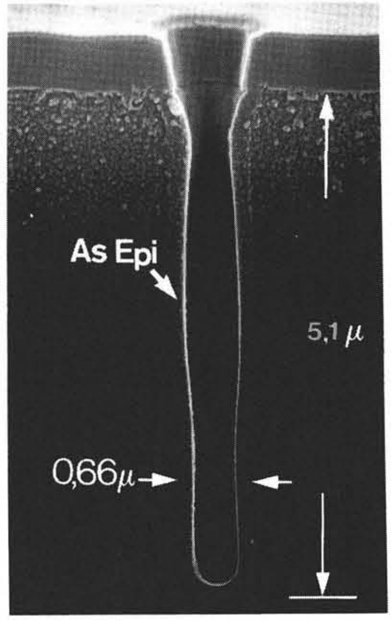

Fig.2: As Epi (0.12 μm, $5x10^{18}cm^3$As) in 5.1 μm deep trench with 0.7 μm diameter. Planar surface is covered with TEOS-oxide. The cleaning process has rounded off trench bottom and upper trench corner.

Technological results on a further doping technique (ref.3) via As doped oxide based on the decomposition of Tetraethylorthoarsenit TEAs are reported elsewhere (ref.4)

Substrate		Structure	Breakdown Voltage at 60 μ A/cm^2	Yield 10mA/cm^2 500ms
0.5-2 μm	As Epi	planar	13 V	96 %
0.25 μm	As Epi	"	12.9 V	90 %
0.12 μm	As Epi	"	12.9 V	91 %
p-2 cm CZ	non Epi	"	12.5 V	58 %
0.15 μm	As Epi		4.8 V	64 %
p-20 cm FZ	non Epi		9.6 V	94 %

Table 1: Oxide quality of 13.5nm SiO_2 on As Epi for planar (8mm^2) and trench structures (1x1x5 μm^3, 2.5mm^2 active area)

Since gate oxide quality for thin Epi is critical, breakdown voltages (60 μA/cm^2) and yields (10mA/cm2 for 500ms) were measured for different As Epi thicknesses on planar structures. Yields were over 90% (see table 1) and better than reference CZ-wafers. As Epi in the trench showed 64% yield but had reduced breakdown voltages presumably because the gate oxide crosses Epi layer/substrate interface on the planar capacitor part.

III. Electrical Characterization

In order to test electrical properties of the different doping techniques test structures were made on p type 0.6-5 Ω cm substrate. 8K cell arrays were made for C(V) measurements with trenches having cross sections of 1x1.25 μm^2 and depths of 3-4 μm. To characterize the electrical isolation between trenches structures consisting of interleaving combs separated by LOCOS isolation were used. Different spacings between adjacent trenches were achieved by varying the trench to LOCOS distance and the width of the field oxide transistor. Trenches had cross sections of 1x3 μm^2 with the longer side face to face.

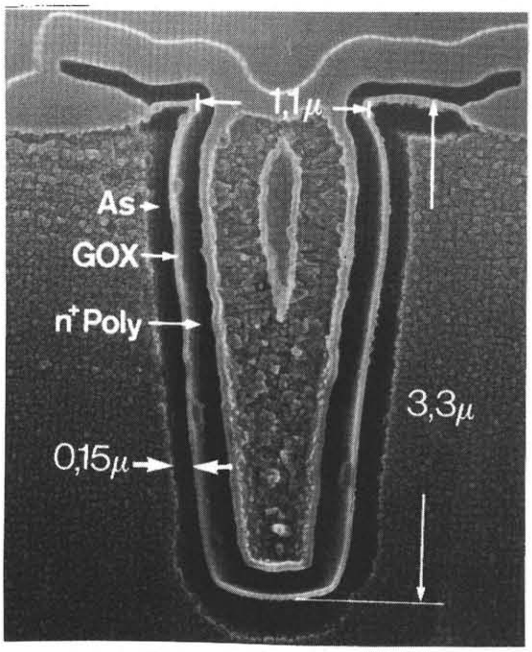

Fig.3: SEM cross section of trench from 8K array. The n^+ doped regions (As SOG, N_2/O_2=9:1, 1000°, 60') are selectively etched.

Fig. 3 shows a SEM cross section of a trench from 8K cell array. Capacitor oxide of 14nm was grown at 900° followed by n^+ Poly-electrode and undoped Poly-Si refill. The n^+ doped regions have been selectively etched in Fig. 3.

Fig. 4 shows a schematic cross section of a test structure for punch through measurements. Each comb of trenches is connected to a highly doped As implanted region to which the test voltage is applied. C(V) curves for P LTO and 1000° As SOG doped trenches show a ratio r= C(-2.5V)/C(+2.5V) of $r \geq 0.95$ while for 950° As SOG the ratio is only 0.8. For As ion implantation r is 0.8 for the trench of Fig. 5 while for trenches like in Fig. 3 it falls below 0.5 demonstrating a strong dependance on trench shape.

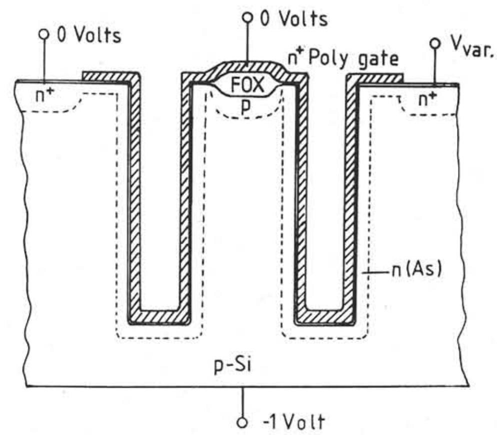

Fig.4: Cross section of punch through test structure (5 μm deep trenches of 1x3 μm^2 with 3 μm side face to face)

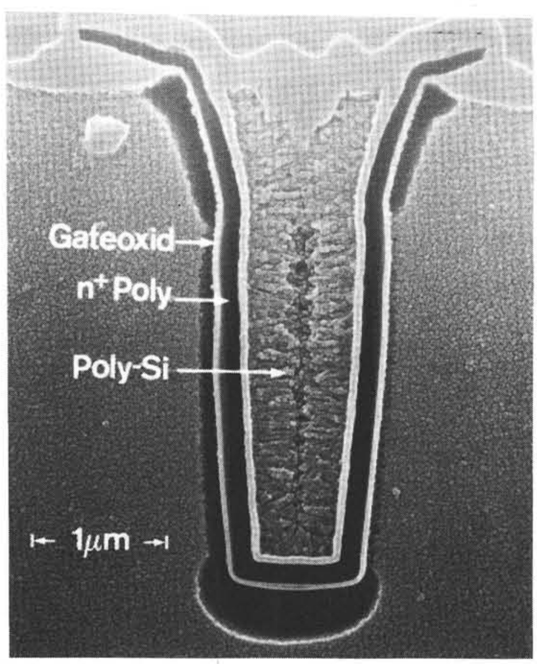

Fig.5: SEM cross section of trench from 8K array with direct Arsenic implantation of $3x10^{15}cm^{-2}$ at 80keV (no screening oxide, drive in 1000°,N_2, 60' with O_2 ramping). The As-beam was inclined by 7° to the left.

Results of punch through measurements are shown in Fig. 6

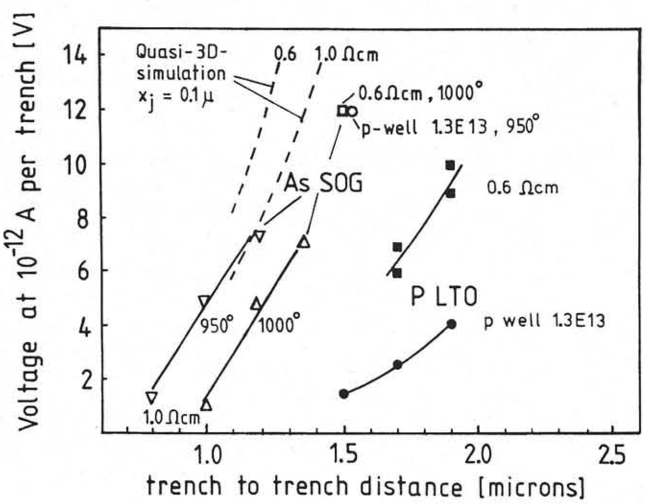

Fig. 6: Voltage at 10^{-12}A trench to trench leakage current versus minimum trench to trench distance. Open symbols are for AsSOG, closed symbols are P-LTO results. Different substrates are indicated in the figure.

Substrate of 0.6 Ωcm and 1 Ωcm with channel stop implantation of $3.10^{13}cm^{-2}$ was analyzed. Tests were also carried out on 5 Ωcm substrat with an additional p-well implant of $1.3x10^{13}cm^{-2}$ at 150 keV followed by an anneal step of 600 minutes at 1150°C. Trenches were doped with As SOG and P-LTO. Punch through voltage was determined at 10^{-12}A leakage current per trench. Due to the very wide outdiffusion of Phosphorous the P-LTO samples exhibited very low punch through voltages. Samples with As SOG show improvement which agrees well with what can be expected from measured junction depths (Fig.1). The difference between samples with As SOG driven in at 950°C and 1000°C corresponds to 0.2 µm in minimum trench to trench distance. Also shown in Fig. 6 are results of simulations (ref. 5) These simulations are two dimensional device simulations carried out in a plane parallel to the silicon surface, where special consideration has been given to the lateral dimensions and shape of the trench. Simulations are in qualitative agreement with the punch measurements.

From Fig. 6 it is evident that for As SOG doped trenches with a minimum separation of 1.4 µm punch through occurs at voltages ≥6V when substrate ≤1Ωcm is used.

IV. Conclusion

With the P and As trench doping techniques presented, threshold voltage shift requirements for mid-level-cell concept are fulfilled e.g. surface impurity concentrations of $5x10^{18}-10^{20}cm^{-3}$ can be obtained. Punch through measurements show that only As doping profiles are shallow enough to prevent punch trough at relevant 4Mbit trench to trench distances of 1.5 µm.

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