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On-Chip Supply Voltage Conversion System and Its Application to a 4Mb DRAM

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An on-chip supply voltage conversion system for VLSI DRAMs, which realizes supply voltage reduction in whole RAM circuits, is newly proposed and applied to a 4Mb DRAM. Implementing the system on a DRAM, short channel MOSFETs could be utilized, thus achieving much faster access time than a DRAM using conventional long channel MOSFETs. The system has been successfully demonstrated to be effective for high density and high speed DRAMs.

1. Introduction

Reliability degradation of MOS transistors due to hot carriers is a serious problem for VLSI memory development. In order to realize high density, high speed DRAMs without sacrificing submicron MOSFET reliability, an on-chip voltage reduction technique is indispensable. Previously, several voltage reduction techniques have been proposed [1-3]. However, all of them were designed to limit the voltage level within cell arrays exclusively. Thus, external Vcc was applied directly to the peripheral circuits, requiring them to be designed with fairly long channel MOSFETs.

In this paper, a new on-chip supply voltage conversion system (VCS), which supplies a reduced voltage to the entire RAM circuits except data out buffers, and its application to a 4Mb DRAM [4] will be presented. By using shorter channel transistors than those of a conventional design, along with the on-chip VCS, an even faster access time was observed.

2. Design concept of the VCS

A new design concept was introduced to fulfill the requirements for VCS; that is 1) to supply a stable internal voltage, and 2) to operate at low power dissipation level. To prevent peripheral circuit operation from being influenced by supply voltage bounce caused by a large momentary current due to bit line charging, two exclusive converters and wirings are implemented. That is to say, one is used exclusively for bit line charging and the other is used for the peripheral circuits. Data out buffers are directly driven by external Vcc to ensure high enough output

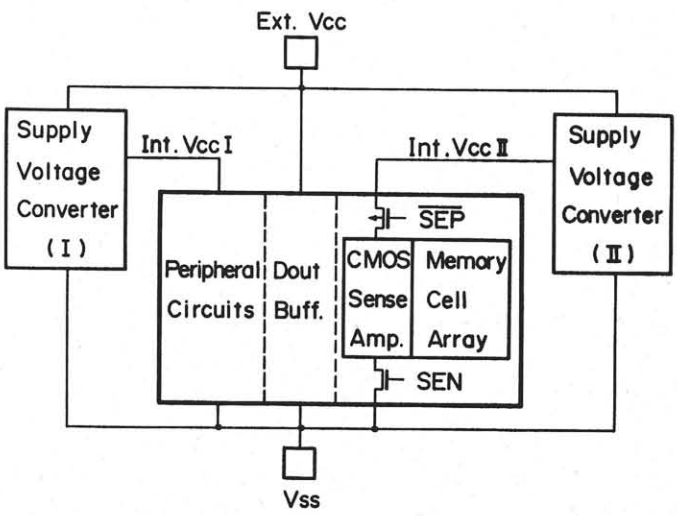

Fig.1 On-chip supply voltage conversion system (VCS) diagram. Supply voltage converter (I) is used for the peripheral circuits and (II) is used for bit line charging.

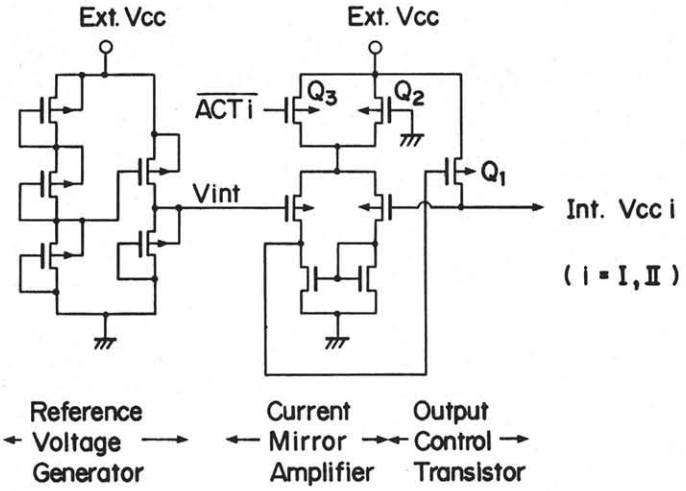

Fig.2 Equivalent circuit of the voltage converter.

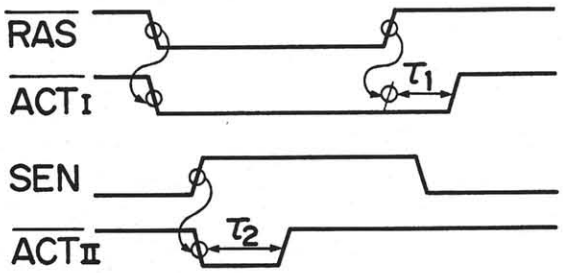

Fig.3 Clock timing diagram for $\overline{\text{ACTI}}$ and $\overline{\text{ACTII}}$. SEN is an internal clock which activates the sense amplifiers. $\overline{\text{ACTI}}$ and $\overline{\text{ACTII}}$ are control clocks to activate the voltage converters.

level. Voltage level shift circuits are inserted between the data out buffers and the other circuits.

The block diagram of the on-chip VCS is shown in Fig.1. The two converters (I) and (II) are feedback type constant voltage regulators, composed of a reference voltage generator, a current mirror amplifier, and an output control transistor Q1, as shown in Fig.2. The reference voltage generator has a constant output (Vint) of 3.5V, independent of the external Vcc. The current mirror amplifier compares the drain voltage of Q1 with the reference voltage, Vint, and controls the conductance of Q1 to keep both voltages equal.

Fast response is very important for such a feedback type regulator since the load impedance can change rapidly. As the current through the amplifier increases, so does the circuit response speed. To realize fast response and low power consumption, a timely activation method was included. The current mirror amplifier has two load transistors as shown in Fig.2. The smaller transistor, Q2, is always ON and the other transistor, Q3, which has larger conductance, is turned on by an internal clock, $\overline{\text{ACTi}}$ (where i=I or II), when the amplifier need to have a fast response time. The clock timings for $\overline{\text{ACTI}}$ and $\overline{\text{ACTII}}$ are shown in Fig.3. SEN is an internal clock which activates the sense amplifiers. $\overline{\text{ACTI}}$ is low while the peripheral circuits are operating, and $\overline{\text{ACTII}}$ is low while bit lines are being charged. The periods T1 and T2 are internally determined.

3. Implementation for a 4Mb DRAM

This VCS was applied to a 4Mb DRAM fabricated using 0.7μm gate n-channel and 1.1μm gate p-channel transistors. Fig.4 shows a photomicrograph of the converter circuits implemented in the 4Mb DRAM. The circuits are placed next to an external Vcc pad. The converter circuit area is as small as 0.2mm^2 which is 0.15% of the total chip area. Measured and simulated DC conversion characteristics of the RAM are shown in Fig.5. The two internal supply voltages Int.VccI and Int.VccII show similar characteristics. It is also seen

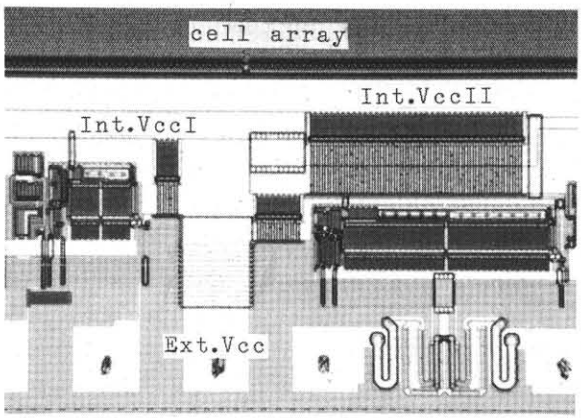

Fig.4 Photomicrograph of the converter circuits implemented in the 4Mb DRAM.

that the voltage reduction characteristics are fairly constant for a wide external Vcc range. Fig.6 shows the dynamic operating waveforms of Int.VccI, Int.VccII and the load current Icc for the RAM. The Int.VccI level variation is as small as 0.4V, while that for Int.VccII is rather large, 0.8V occurring, when bit lines are being charged. However, it should be noted that the Int.VccII bounce does not influence the Int.VccI level, i.e. the peripheral circuit operation. Since a timely activation method of the converters is introduced, the power consumption of the VCS is limited to 2mW in standby mode and 15mW in minimum cycle operation.

The RAS access time of the RAM is shown as a function of external Vcc by the solid line in Fig.7. The dependence of the access time on the external Vcc level in the high voltage region is caused by both the small dependence of the internal Vcc and the dependence of data out buffer speed on the external Vcc level. As a reference, another 4Mb DRAM, which operates under external Vcc, was fabricated using a different metal mask

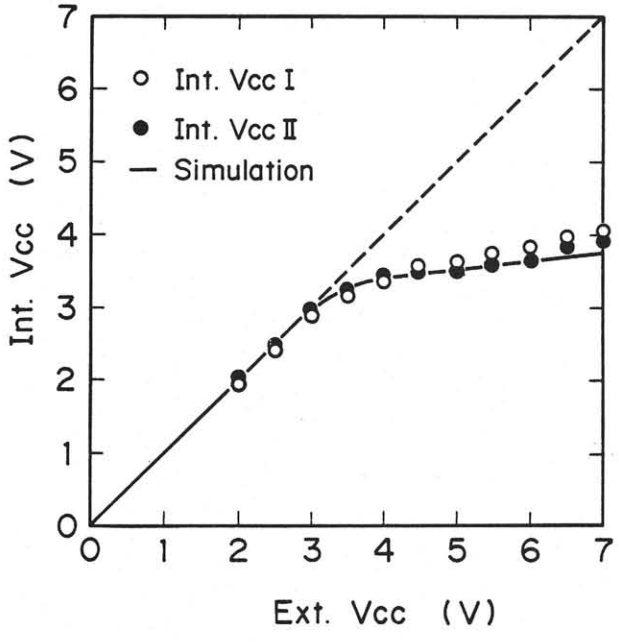

Fig.5 DC conversion characteristics for the on-chip VCS implemented in the 4Mb DRAM.

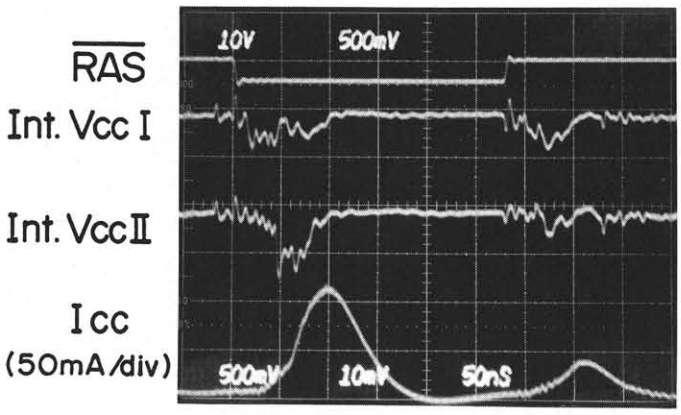

Fig.6 Operating AC characteristics of the internal Vcc and Icc.

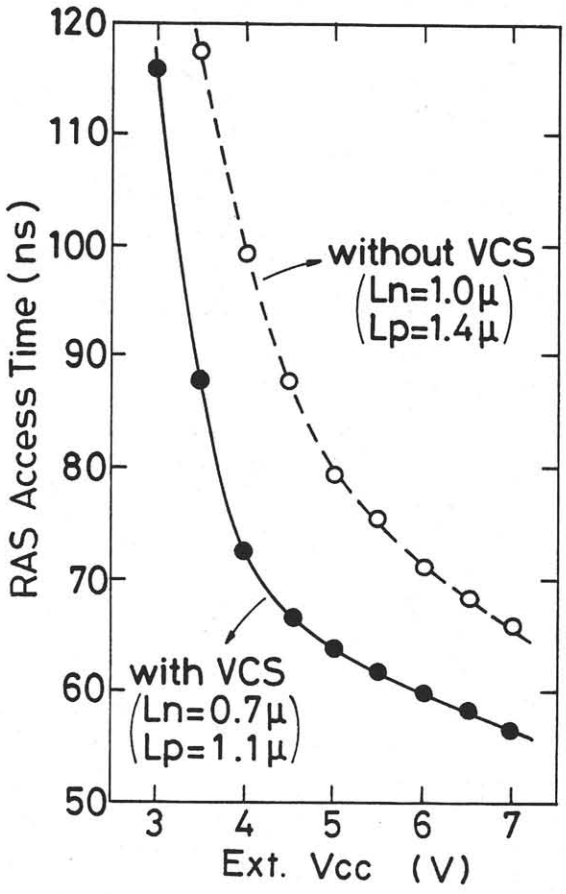

Fig.7 Solid line shows a measured RAS access time of a RAM fabricated with 0.7μm gate n-channel transistors and 1.1μm gate p-channel transistors using the converter function. The broken line shows that of a RAM fabricated with 1.0μm gate n-channel transistors and 1.4μm gate p-channel transistors bypassing the converter function.

which allows for the VCS circuits to be bypassed. To ensure MOSFET reliability, this RAM was composed of longer channel MOSFETs, 1.0μm and 1.4μm for n-channel and p-channel, respectively. The RAS access time of this RAM was also measured and is shown in Fig.7. The RAM composed of shorter channel MOSFETs operating under internally converted Vcc has demonstrated to achieve faster access time than one composed of longer channel MOSFETs operating under external Vcc.

An internally converted supply voltage level should be chosen considering the MOSFET reliability as well as circuit operating characteristics. Fig.8 shows the degradation in drain current of n-channel MOSFETs after 10^4 sec DC stress, as a function of gate length with drain voltage (Vd) as a parameter. When the drain voltage is below 5V, the degradation is negligibly small. It is said that a little reduction of the drain voltage greatly improves the transistor reliability.

The maximum operation voltage of the conventional DRAM with boosted word lines is beyond 7V, while one with the VCS can be limited to below 6V. Therefore, the RAM composed of 0.7μm gate transistors with the voltage reduction system can be expected to have better reliability than one composed of 1.0μm gate transistors operating under external Vcc.

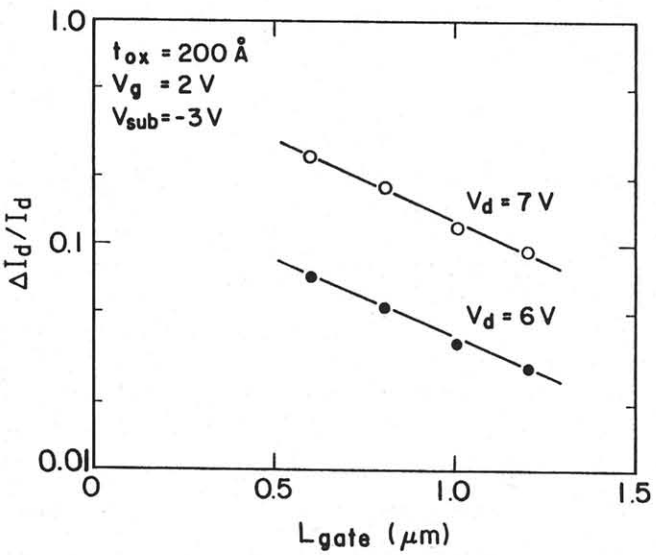

Fig.8 Degradation in drain current of n-channel MOSFETs as a function of gate length with drain voltage as a parameter. The stress time is 10^4 sec.

4. Conclusion

An on-chip supply voltage conversion system for VLSI DRAMs has been newly proposed and applied to a 4Mb DRAM. The system allows short channel MOSFETs to be used for the DRAM design obtaining both a faster access time and a high reliability than a DRAM using conventional long channel MOSFETs with external Vcc supply. The system was successfully verified to be effective for high density and high speed DRAMs.

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