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High-Density CCD Video-Memories: Physics and Technology

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Investigations of high-density Charge-Coupled-Device memory structures for Megabit video-memories, as a follow-up of the 308 Kbit video-serial-memory [1], are presented.

A new technology for making submicron grooves in a polysilicon layer will be described. It is used for fabricating an experimental 100 Kbit CCD memory with a cell size of $3*3.5\ \mu m^2$.

Scaling of CCD-memory cells down to $1\ \mu m^2$ is not limited by charge storage (as it is for DRAM cells), but by lithography. Several physical phenomena involved in down-scaling, e.g. hot electrons and inter-electrode potential barriers, will be discussed.

INTRODUCTION

CCD memories are particularly suited for video and audio applications because of the serial data stream. Compared to DRAM's they have two major advantages: the cell size is much smaller and they can be scaled down much further.

The cell size of a conventional CCD structure is about $8L^2$ (where L is the minimum dimension) and in the PABLO-technology [2] (see next section) the cell is only $4L^2$. That is 4 to 6 times smaller than for a DRAM cell [3].

Because of the large signal loss along the bitline capacitance, which does not scale with the cell size, the storage capacitance in a DRAM must be kept at a more or less constant value of 35 to 60 fF. Together with a minimum gate oxide thickness of 100 Å this results in a minimum DRAM cell of about $30\ \mu m^2$. This is illustrated in fig. 1. Here is assumed that the storage area is ⅓ of the cell area. In a CCD memory the minimum charge packet is determined by a much smaller parasitic capacitance because the sense amplifier is laid-out within several microns from the last storage capacitor. The signal loss is therefore much less and the CCD memory can operate with 20 to 40 times smaller charge packets. As an example: the 100Kbit CCD memory (see next section) operates with a storage capacitor of about 2fF. Because of this property a CCD cell can be scaled down much further (say to $1\ \mu m^2$) without the need of trenches as for DRAM's.

TECHNOLOGY

Perfect-Alignment-By-Lateral-Oxidation (PABLO) is a new technology for making submicron grooves in a polysilicon layer [2]. The key feature is to use the submicron width of the oxide rim, formed by lateral oxidation of a second polysilicon layer, as a definition for the grooves to be etched in the underlying first polysilicon.

Details of the process-flow are described in fig. 2. The final structure consists of coplanar polysilicon electrodes isolated by oxidized submicron grooves and alternately covered by oxide and nitride. The width of the groove is accurately controlled in the range of 0.1 to 0.8 μm by the lateral oxidation process. Because the alignment tolerance between the electrodes is eliminated, the cell size is only $4L^2$.

In a standard 1.5 μm-250 Å NMOS-process, and using PABLO, a 100Kbit memory (cell size $3*3.5\mu m^2$) was made on 20 to 30 Ohm.cm p-type silicon. The gate structure is shown in fig. 3 and compared with the conventional overlapping gate structure [1]. The memory has the well known serial-parallel-serial structure as schematically is given in fig. 4. The data is interlaced in the parallel registers and clocked with an 8-phase ripple clock. There were no problems with charge transfer over the gaps. The absence of inter-electrode potential barriers during charge transfer is in agreement with two-dimensional numerical simulations (see fig. 5). This figure shows the electrostatic potential distribution along the interface. If 5 Volt is applied at electrode B the potential barrier(due to − 2.5 Volt substrate bias) is drawn away by the lateral electric field (curve ②). If a charge packet is stored in the potential well, the surface potential becomes lower; curve ③ corresponds with an electron density of 3.10^{12} electrons/cm^2, which is about 3.3 Volt. This agrees well with the measured maximum signal voltage of 3 Volt.

The measured charge transfer-loss (see fig. 6) is remarkably low for these surface-CCD's due to the high density of stored charge and the low interface states density (Nss ~ 5.10^8 cm^{-2}).

The CCD-channels are not isolated by LOCOS, but by a boron-implantation only. This reduces the cell area needed for isolation and nearly doubles the effective storage area of the cell. The boron-dose must be chosen carefully because measurements show that the leakage current, generated at the interface, increases strongly with the dose at higher gate-substrate bias (fig. 7). A dose of 1.10^{13} cm^{-2} is still acceptable concerning leakage and yet sufficient as an isolation barrier between the CCD-channels.

PHYSICS

Down-scaling of the more conventional overlapping gate-structure has also been investigated. Three physical phenomena have to be considered in particular: inter-electrode potential barriers, barrier-lowering between successive potential wells and impact-ionization (fig. 8).

Potential barriers at the gap can degrade strongly the charge transfer. For small gaps and not too high impurity concentrations these potential barriers are drawn away by the lateral electric field and complete charge transfer is possible. On the other hand however, the gap must not be made too small in order to prevent avalanche due to the high electric field. From two-dimensional calculations we have determined quantitatively the conditions necessary for safe operation: charge transfer not impeded by potential barriers and electric fields smaller than 2.10^5 V/cm (see fig. 9).

Fig. 10 shows the calculated lateral electric field between the storage electrode(5 V., 10 V.) and the transfer electrode (0 V.). The gap is 0.2 μm. If charge is transferred through this high-field region, avalanche multiplication does increase the electron charge packet while the extra holes flow to the substrate. In fig. 11 the output signal of a CCD structure with 400 gates is measured for resp. 5 V., 8 V. and 10 V. drop clocks. If a push clocking scheme is used, the charge packet does not endure such a large potential differences during transfer and no avalanche multiplication could be measured for these clock voltages. This illustrates that not only the cell structure but also the clocking scheme has to be optimized.

Acknowledgments

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[1] M.J.M. Pelgrom e.a. *"A digital field memory for TV-receivers"*, IEEE Cons. El. Conf., June 1983 Chicago; and H.J.M. Veendrick e.a. *"A 40 MHz 308 Kb CCD Video Memory"*, ISSCC 84, Feb. 1984.

[2] H.G.R. Maas, J.A. Appels, Phil. J. Res. 103-108; and U.S. Patent 449287.

[3] S. Asai, *"Trends in Megabit Drams"*, IEDM 84.

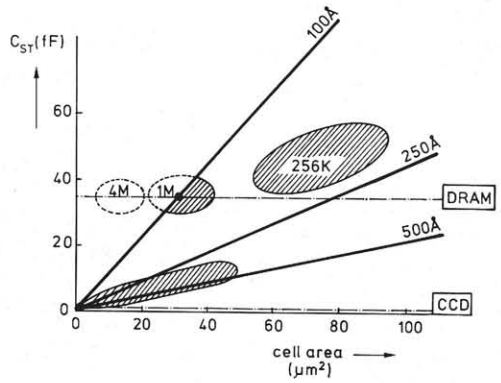

Figure 1.
CCD memories can operate with a much smaller storage capacitance (C_{ST}) than DRAM's. Straightforward downscaling is limited by tunnelling through the gate oxide ($\approx$ 100 Å gate oxide thickness). For a DRAM the critical cell area is about 30 μm^2 and for a CCD cell only 1 μm^2.

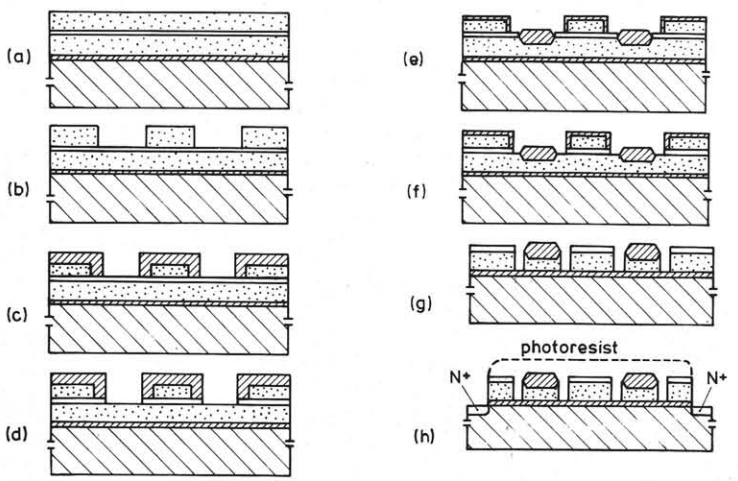

Figure 2.
a) The starting structure is a sandwich of a phosphorus-doped silicon layer (P1), a CVD Si_3N_4 layer and an undoped polysilicon layer (P2) on top of 250 Å gate oxide; b) definition of P2; c) oxidation of P2 (the lateral thickness of this oxide defines later on the submicron width of the groove); d) the exposed parts of Si_3N_4 are etched; e) dip etch of oxide; selective oxidation of P1 and P2; f) the exposed parts of Si_3N_4 are etched away giving access to P1; g) etching of the grooves in P1 (the remaining P2 is etched simultaneously); h) definition of source/drain regions.

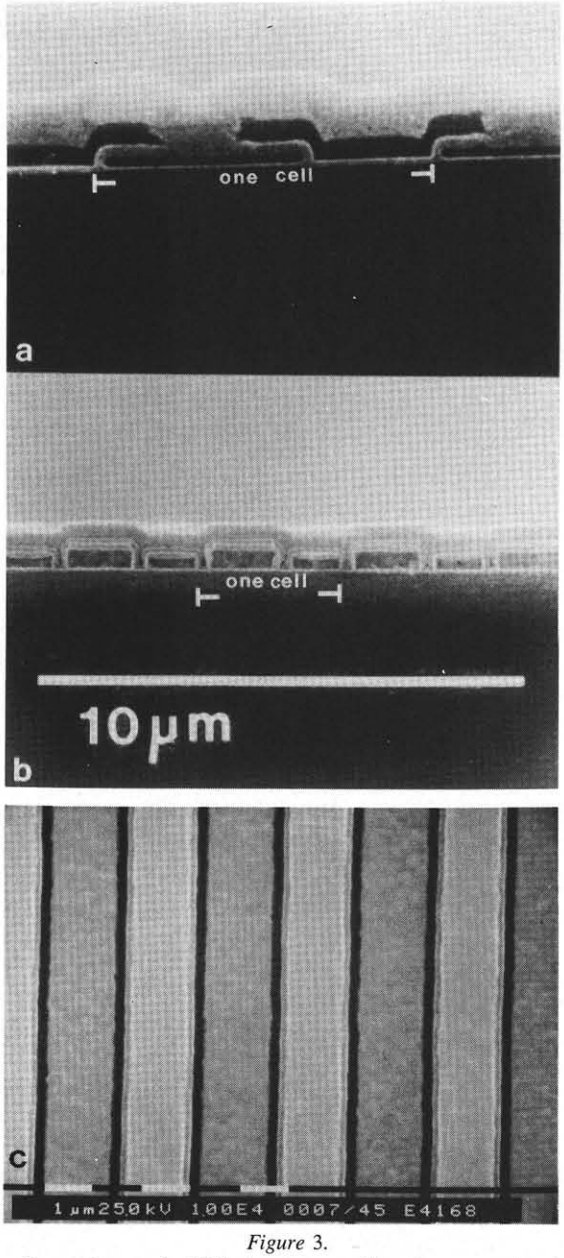

Figure 3.
Comparison of CCD-structures with a) conventional overlapping electrodes for a 2 µm-process and b) PABLO-electrodes for a 1.5 µm-process. c) Top view of PABLO-gates.

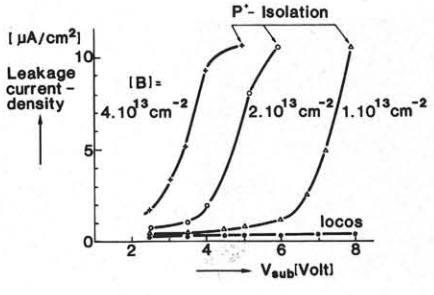

Figure 7.
Leakage current density at 90° C as a function of the gate to substrate Voltage for different boron-doses. For LOCOS-isolation no increase with substrate voltage is shown.

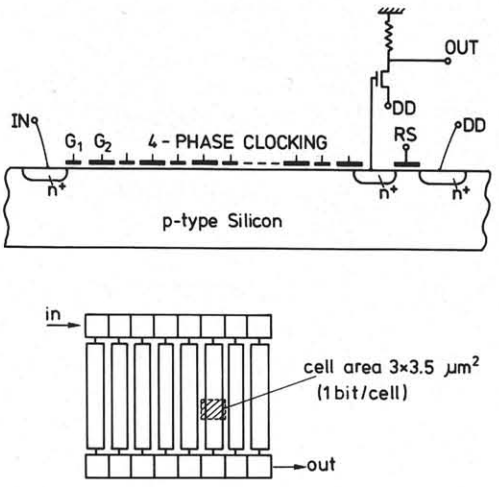

Figure 4.
Schematic cross-section of CCD-register and SPS CCD memory structure.

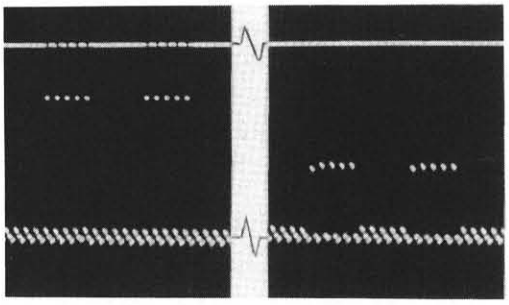

Figure 6
*Measured input (upper trace) and delayed output pulses (lower trace) of 100 Kbit memory block with 3 * 3.5 µm² cell size; the vertical scale is 500 mV/sd.*

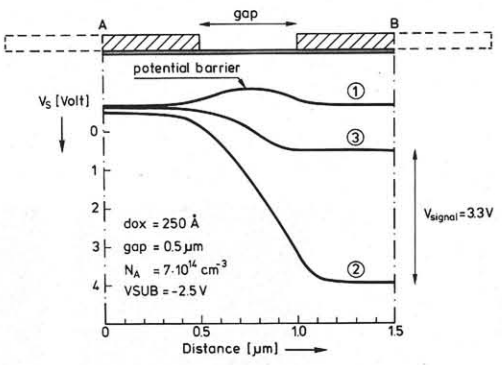

Figure 5.
Calculated surface potentials for 1 µm gates with 0.5 µm gaps; V_A = 0 Volt; for curves ① and ② the electron charge density is zero and V_B is resp. 0 Volt and 5 Volt; for curve ③, V_B = 5 Volt and the electron charge density is 3.10^{12} el./cm².

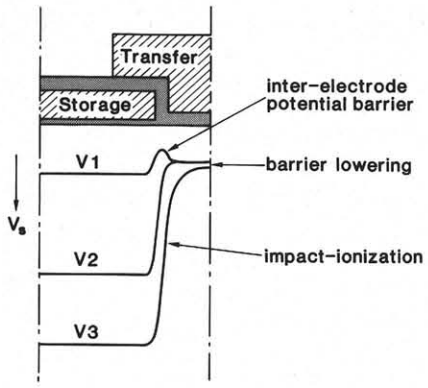

Figure 8.
Surface potential distributions for three voltages of the storage-gate illustrate the relevant physical phenomena.

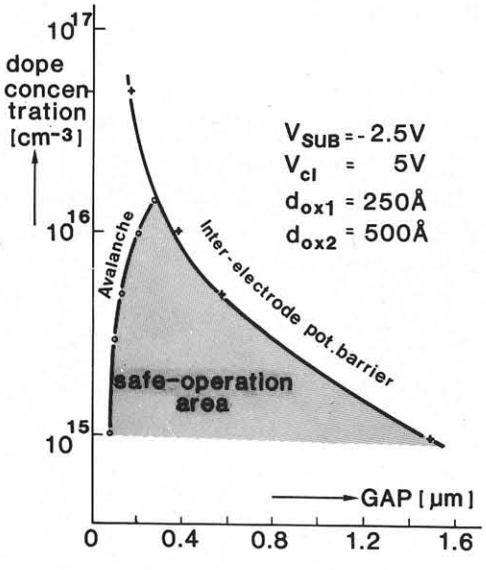

Figure 9.
For substrate impurity concentrations and gap sizes in the "safe-operation-area" no-interelectrode potential barrier is present and the maximum electric field is less than 2.10^5 *V/cm, which is used as an indication of avalanche multiplication.*

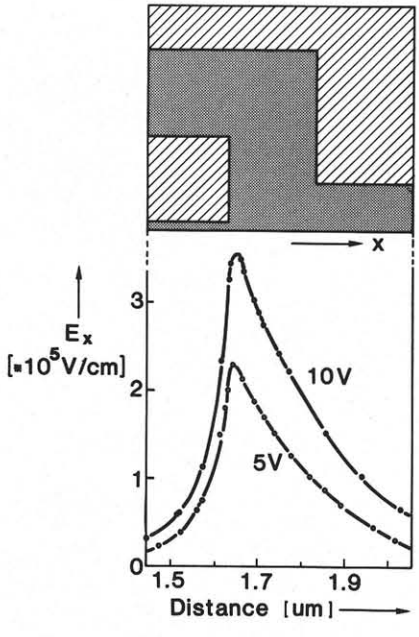

Figure 10.
2 D-calculated lateral electric field in the gap-region for 5 V and 10 V clock voltage.

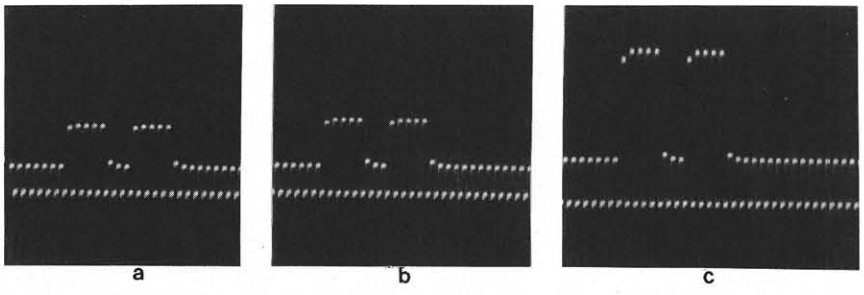

Figure 11.
Impact ionization increases the CCD-output signal (200 mV/sd) for higher clock voltages: a, b,c correspond with 5 V, 8 V and 10 V clock voltage.