Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 319-322

B-7-3

A 7 ns/350 mW 16Kb Hi-BiCMOS Static RAM

Makoto SUZUKI, Hisayuki HIGUCHI, Suguru TACHIBANA,
Atsuo WATANABE*, Takahide IKEDA*, and Masanori ODAKA**

Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185
*Hitachi Research Laboratory, Hitachi Ltd., Hitachi, Ibaragi 319-12
**Device Development Center, Hitachi Ltd., Ohme, Tokyo 187

An experimental ECL 16Kb static RAM is developed with a typical address access time of 7ns, typical power dissipation of 350mW and 8.5mm^2 chip size. These performance levels are achieved by using 1.3μm Hi-BiCMOS (High performance BiCMOS) technology[1] and optimizing the common data line signal swing in order to reduce the related delay time.

1. Introduction

Recently, intensive efforts have been made to achieve high speed, high density static RAMs, which are key components in high performance systems. By developing new circuits and scaling down device structures, it has been possible to realize MOS static RAMs that attain such performances. However, most high speed applications have been left to bipolar static RAMs. As a result, attention has turned to BiCMOS static RAMs, since they feature both the high speed characteristics of bipolar transistors and the low power advantage of CMOS FETs. 64Kb static RAMs[2)3)] with a typical address access time of less than 15ns have been fabricated using 2μm Hi-BiCMOS (High performance BiCMOS) technology.

This increase in speed has been achieved by using high-sensitivity, high-speed bipolar sense amplifiers, and high-speed bipolar-CMOS combination gates (BiCMOS gates) in peripheral circuits. To increase speed further, however, it is essential to investigate the acceptable minimum read signal swing on the common data line to reduce the related delay time. By utilizing its measured value, an ECL 16Kb test chip was designed and fabricated using 1.3μm Hi-BiCMOS technology.[1] The resultant high speed characteristics of this static RAM are described below.

2. Device and BiCMOS gate characteristics

A cross-section of the 1.3μm Hi-BiCMOS device is illustrated in Fig. 1. Bipolar transistors and CMOS FETs are fabricated in an epitaxial layer with buried layers, without degrading the characteristics of either device as performed in bipolar and CMOS LSIs, respectively. The structure involves double level polysilicon and double level aluminum metallization. Major device characteristics are listed along with those of a 2μm device in Table 1 for comparison. Cutoff frequency f_T of the bipolar transistor is improved to 6GHz, 1.5 times that of the 2μm device, and the β_{omax} values of the MOS FETs are also improved by about 1.7 times.

The performance of the BiCMOS gates, along with that of the CMOS gates designed to occupy the same gate area, is shown in Fig. 2. The propagation delay time at 1pF load capacitance with the BiCMOS gate is reduced from 0.8ns for the 2μm device[4] to 0.5ns for the 1.3μm device. This propagation delay time improvement ratio, the square root of $f_T \times \beta_{omax}$ improvement ratio, is in good agreement with the analytically predicted value.[5] As for the CMOS gate, the same propagation delay time improvement ratio is obtained, because this ratio is equal to the β_{omax} improvement ratio. Thus, the 1.3μm Hi-BiCMOS

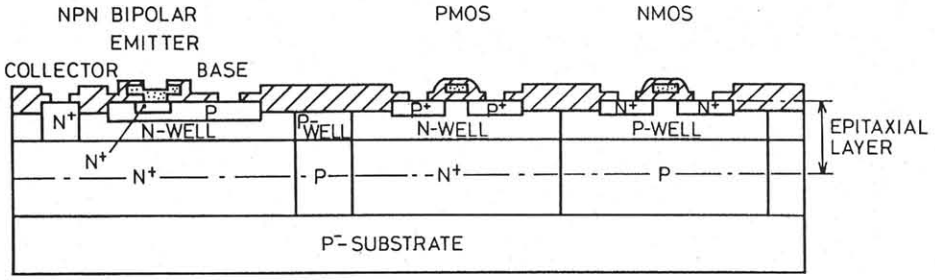

Fig. 1 Cross-section of the 1.3μm Hi-BiCMOS device.

Table 1 Hi-BiCMOS device characteristics.

Device	Characteristics	Value		Unit
		2μm device	1.3μm device	
Bipolar	Emitter	2X3	1X2	μm^2
	h_{FE}	100	86	—
	BV_{CEO}	8.6	8.0	V
	R_{CS}	100	180	Ω
	f_T	4	6	GHz
NMOS	V_{TH}	0.55	0.58	V
	β_{omax}	50	80	μS/V
PMOS	V_{TH}	-0.55	-0.52	V
	β_{omax}	15	27	μS/V

gates permit to operate two times faster than the 1.3μm CMOS gates, the same as the case of 2μm Hi-BiCMOS technology.

3. Static RAM circuit design

An ECL 16Kb static RAM test chip was designed and fabricated using the 1.3μm Hi-BiCMOS devices described above. A schematic diagram of the memory cell and peripheral circuits of the data line and common data line is shown in Fig. 3.

The input buffer circuit[3] consists of a bipolar ECL reciever and the BiCMOS gates. The bipolar ECL reciever detects the ECL level small input signal. The BiCMOS gates are also used in the word driver, decoder and control circuits to drive large capacitive loads. The memory cell is a cross-coupled four-NMOS flipflop with two high-resistance polysilicon loads and a polycide Vss-line[6] measuring 104μm^2.

The signal swing on the common data line, which has a slow transition time due to parasitic capacitances, is a parameter of vital importance in achieving fast access time as the integration

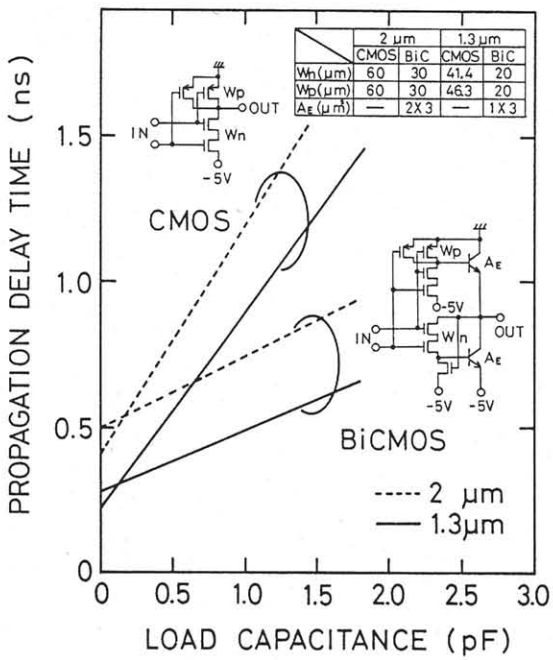

Fig. 2 Experimental propagation delay time of CMOS and BiCMOS 2 input NAND gates.

level increases. The response of the common data line differential voltage $\Delta v_{CD}(t)$ is expressed as

$$\Delta v_{CD}(t)=\Delta V_{CD} \times\left\{2e^{-\zeta\omega_n t}\left(\cosh\omega_n\sqrt{\zeta^2-1}\,t+\frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\omega_n\sqrt{\zeta^2-1}\,t\right)-1\right\}$$

$$\Delta V_{CD}=\frac{R_1R_2R_3I}{R_1+R_2+R_3}$$

$$\omega_n=\sqrt{\frac{I}{\Delta V_{CD}R_2C_DC_{CD}}}$$

$$\zeta=\frac{1}{2\omega_n}\left(\frac{R_1+R_2}{R_1R_2C_D}+\frac{R_2+R_3}{R_2R_3C_{CD}}\right)$$

where R_1, R_2, R_3 are the resistances of the data line load NMOS FET (Q_{nL}, $\overline{Q_{nL}}$), Y switch NMOS FET (Q_{nY}, $\overline{Q_{nY}}$), and common data line load NMOS FET (Q_{nC}, $\overline{Q_{nC}}$), respectively. I is the memory cell read current and C_D and C_{CD} are the parasitic capacitances of the data line and common data

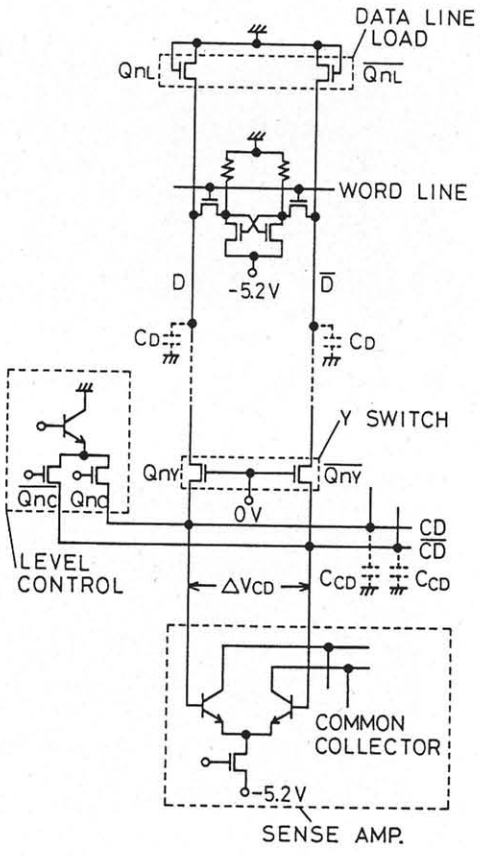

Fig. 3 Schematic diagram of memory cell and peripheral circuits of the data line and common data line.

line, respectively. ΔV_{CD} represents the common data line signal swing. Speed of the response is determined mainly by the angular frequency ω_n and by the decay constant ζ.

Figure 4 shows the propagation delay time dependence on the common data line signal swing ΔV_{CD}. The dashed line represents analytically calculated results using the equations described above, the solid line shows simulated results. The propagation delay time from the word line to the common data line is reduced almost linearly with a decrease in the common data line signal swing ΔV_{CD}. Therefore, bipolar differential sense amplifiers, which are able to detect a small ΔV_{CD}, were adopted to obtain higher speed. As shown in Fig. 4, the delay time from the common data line to data output is almost independent of the ΔV_{CD} value. Thus, faster access time can be realized by decreasing the common data line signal swing.

The data line voltage is affected by the NMOS

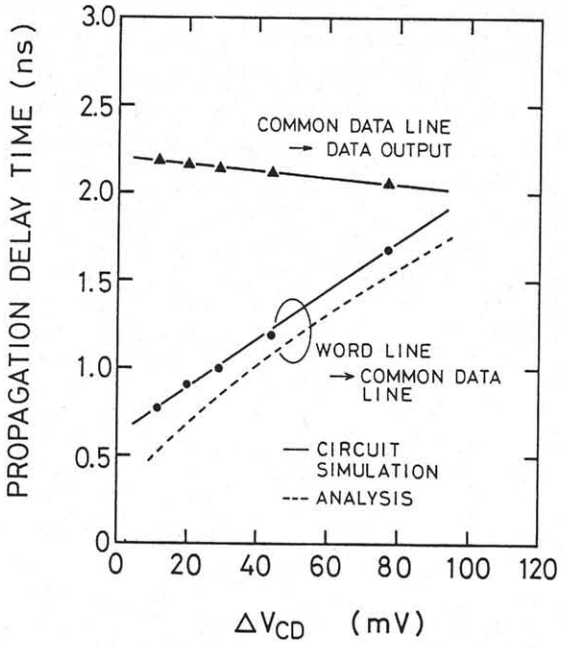

Fig. 4 Propagation delay time dependence on the common data line signal swing, ΔV_{CD}.

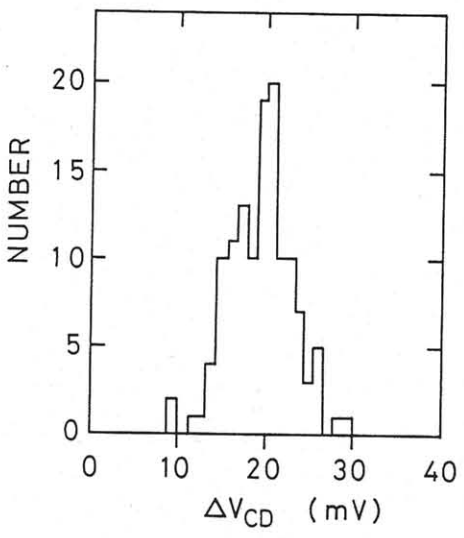

Fig. 5 Differential read voltage variations on the common data line.

data line load threshold voltage (V_T) in this circuit. As a result, a detrimental differential voltage may develop on the pair of data lines D and $\overline{D}$, as well as on the common data lines CD and $\overline{CD}$. This differential voltage is due to the V_T mismatch occurring in the data line load transistors. It is this problem that determines the acceptable minimum common data line signal

swing. The measurements of differential read voltage variations on the common data line are shown in Fig. 5. In this case, the average read signal is about 20mV while the actual read signal ranges between 10 and 30mV. Since the bipolar sense amplifier (Fig. 3) can detect a 5mV differential signal, this 20mV average read signal swing appears to be the acceptable minimum common data line signal swing. By utilizing this value of 20mV for the common data line signal swing, the 16Kb test chip was designed.

4. Performances

A microphotograph of the 16Kb test chip, measuring 2.3×3.7mm^2, is shown in Fig. 6. Waveforms for the chip having a typical address access time of less than 7ns are shown in Fig. 7. Power dissipation at nominal operating conditions (-5.2V, 25°C) is 350mW. Table 2 summarizes the features of the 16Kb test chip.

5. Conclusion

A high performance 16Kb ECL static RAM has been realized using 1.3μm Hi-BiCMOS technology and optimizing the common data line signal swing design. Typical address access time of the RAM is 7ns with a power dissipation of 350mW.

6. Acknowledgements

The authors would like to thank K. Itoh for his helpful suggestions and discussions, T. Nagano and I. Masuda for their arrangements of this work. The authors also would like to thank M. Kubo, K. Ogiue, and S. Asai for their support and continued encouragement.

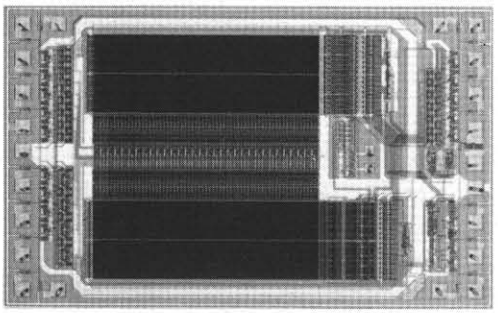

Fig. 6 Microphotograph of a 16Kb static RAM test chip.

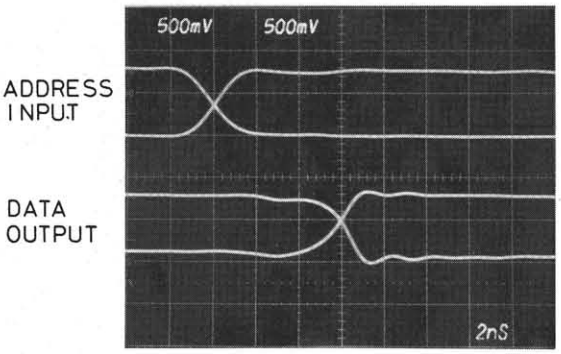

Fig. 7 Address access waveforms.

Table 2 Typical characteristics of the 16Kb static RAM.

Organization	16K X 1 bit
Address access time	7 ns
Power dissipation	350 mW
Chip size	2.3 X 3.7 mm^2
Cell size	104 μm^2
I/O interface	ECL

References

1) A. Watanabe, et al. ; "High Speed BiCMOS VLSI Technology With Buried Twin Well Structure", Digest of IEDM Technical Papers, pp. 423-426, 1985.

2) K. Ogiue, et al. ; "A 15ns/250mW 64K Static RAM", Proceedings of ICCD, pp. 17-20, 1985.

3) K. Ogiue, et al. ; "A 13ns/500mW 64Kb ECL RAM", ISSCC Digest of Technical Papers, pp. 212-213, 1986.

4) Y. Nishio, et al. ; "A Subnanosecond Low Power Advanced Bipolar-CMOS Gate Array" ; Proceedings of ICCD, pp. 428-433, 1984.

5) H. Higuchi, et al. ; "Performance and Structures of Scaled-Down Bipolar Devices Merged with CMOSFETs" ; Digest of IEDM Technical Papers, pp. 694-697, 1984.

6) S. Yamamoto, et al. ; "A 256K CMOS SRAM With Variable-Impedance Loads" ; ISSCC Digest of Technical Papers, pp. 58-59, 1985.