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An EPROM Cell Structure for EPLDs Compatible with Single Poly Gate Process

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A single poly-Si gate EPROM cell structure which eliminates the process complexity of a conventional double poly-Si EPROM technology is proposed to realize EPLDs with a faster turnaround-time. As the proposed cell uses an N^+ diffused layer on bulk Si substrate as a control gate instead of 2nd poly-Si, superior reliability related to bias stress data retention are obtained.This is due to the higher quality of bulk Si oxide compared with an interpoly insulator. Basic cell characteristics(write, erase, I-V, high temperature data retention etc.) are almost the same as those of a double poly cell. It is found that the single poly cell is easily combined with logic's single poly and double metal process, therefore it should be greatly contribute to develop CMOS EPLDs in spite of the cell area increase.

INTRODUCTION

With the rapid development of Application Specific Integrated Circuits(ASICs), CMOS Erasable Programmable Logic Devices(EPLDs) are now receiving more attention. CMOS EPLDs can realize user programmable and reconfigurable logic devices with a faster production turnaround time. Moreover, new devices with more sophisticated AND, OR, NAND and NOR array configurations can be easily developed. Therefore, it should be necessary to combine current CMOS EPROM technology[1)2)] with advanced architectures and circuit techniques. However, most popular logic devices use a single poly-Si and a double metal process. Therefore, the introduction of conventional double poly-Si EPROM technology to a logic process naturally leads to production cost increase and fabrication process complexity, which degrades production yields. Moreover, process technologies[3)] to form reliable interpoly insulator and double poly cell are also indispensable.

This paper describes newly developed single poly-Si gate EPROM cell technology[4)], which uses an N^+ diffused layer on a Si substrate as a control gate(CG) to meet the previously mentioned requirements. As the N^+ layer is additionally formed and used instead of an n-well layer[3)], relatively smaller cell size are realized and the possibility of applications to logic and microproccesors are more increased.

CELL STRUCTURE AND FABRICATION PROCESS

Fig.1 shows a typical cross section of single poly-Si gate cell. The N^+ diffused layer is used for a control gate(CG) which is capacitively coupled to an extended poly-Si floating gate(FG). The top view photograph of the cell is shown in Fig.2. Both the cell transistor channel region and the CG N^+ layer are fabricated on a Si substrate and are electrically isolated each other by a field oxide. Table 1 shows device process parameters of fabricated cells. The process sequence based on 1.2 um NMOS technology with 200A gate oxide is shown in Fig.3. In order to fabricate this cell, only one extra mask step to define CG N^+ layer and an ion implant process has to be added. In this experiment, the gate oxide and CG oxide are grown simultaneously. To investigate the effect of formation of a deep deletion layer in CG on write characteristics, various CG N^+ diffused structures, which are formed by P ion implantation and As ion implantation with higher and lower dosage, are examined.

RESULTS AND DISCUSSION

ELECTRICAL CELL CHARACTERISTICS

Basic write characteristics of the new cell with W/L_{eff} = 1.2um/0.7um are shown in Fig.4.

Essentially, control gate and drain voltage dependences of a write characteristics of the new cell are almost the same as those of the conventional double poly cell, because the

capacitance ratio between CG and channel region and total capacitance determine the cell write properties. In the new cell, since the CG is formed by an N^+ diffused layer, it is likely that the write voltage is limited by the CG N^+ junction breakdown voltage, the turn-on voltage of parasitic poly-gate field transistor and the punchthrough voltage between the CG and the channel region of the cell. Actually, the junction breakdown voltage and threshold voltage of the field transistor are more than 14V, therefore a standard 1.2um EPROMs write voltage, 12.5v, is easily realized.

In order to evaluate the CG N^+ concentration effect on the write characteristics, three structures are examined. Phosphorus ion implant ($5E15cm^{-2}$), arsenic ion implant of higer ($5E15cm^{-2}$) and lower ($2E12cm^{-2}$) dosages are compared to estimate the degradation of Vth shifts after writing due to the formation of a deep depletion layer in CG. About 1V degradation for As dosage of $2E12cm^{-2}$ is observed, as shown in Fig.5. Therefore, it becomes possible to utilize D-type ion implantation for CG layer formation and , in this case , the extra N^+ defined mask and N^+ ion implant process are completely reduced.

Fig.6 shows typical I-V characteristics of the cell. Drain read current Id of 140uA at Vd = 1.5V, which is about 1.5 times of that of the conventional cell, is obtained with a $5.5um^2$ gate coupling area. Essentially, as the channel width and the FG potential determines the drain current, it is possible to gain more read current by increasing the channel width with increasing the CG area to meet the requirement of higher speed operation.

Erase characteristics are shown in Fig.7. Erasing speed is almost 2.8 times faster than that of the double poly cell, which is probably due to the increase of UV irradiated FG perimeter length on the N^+ layer[4)5)]. To maintain this desirable feature, precaution on an actual cell layout is necessary.

RELIABILITY

The most important items on the EPROM reliability are the bias stress data retention[1)3)] and high temperature data retention.

Charge retention characteristics of the new cell by applying positive bias on CG are shown in Fig.8. More than 5 $MVcm^{-1}$ field strength for a single poly-gate cell is obtained, which is about 2 $MVcm^{-1}$ higher than that of a conventional double poly cell with poly-oxide as an interpoly insulator. Below the CG N^+ layer junction breakdown voltage, current leakage is completely suppressed. This feature comes from the use of the bulk-Si oxide on N^+ layer as the CG oxide instead of an interpoly oxide of a double poly cell and the single poly-Si FG structure itself. The leakage field strength of poly oxide is generally lower than that of bulk-Si oxide due to the grown poly-Si surface asperity and the degradation of oxide quality related to defect density increase. The field enhancement at the FG poly-Si edges which are conformaly surrounded by the CG poly-Si extremely reduces the field strength of double poly cell. In case of single poly cell, such problems are completely solved. As a result, no special interpoly insulator(poly-oxide, stacked layer etc.) technology[3)] is needed.

Fig.9 shows data retention characteristics of the single poly-gate cell as a function of temperature. High temperature retention is found to be essentially the same as that of a conventional EPROM cell, because the quality of poly-oxide covering the FG determines the thermionic emission rate of electrons from the floating gate[6)]. About 1eV activation energy was obtained and more than 10 years data retention at 150°C is ensured.

Fig.10 shows a typical example of the cell layout . Control gate and source regions are shared by two cells. An area of the unit cell is about two to three times larger than that of the double poly cell. For example, cell size of about 50 um^2 with 1.2 um design rule are obtained, compared with 20 um^2 of conventional double poly cell. It should be noted that this cell size is applicable not only for the logic and microprocessor field but for medium scale memory devices. In spite of the area increase by use of single poly-gate cell, the proposed cell shows superior reliability and is realized by adding a few extra process steps. Therefore, the introduction of this cell to the logic and

microprocessor field will be promising to develop the ASICs.

SUMMARY

Basic cell electrical characteristics and reliability aspects of the single poly-Si gate EPROM have been described and discussed. It is obvious that only a few extra process steps are necessary to combine this reliable single poly-Si cell with a standard logic and microprocessor process. Therefore, this technology is promissing and will greatly contribute to the development of CMOS EPLDs and ASICs.

ACKNOWLEDGEMENT

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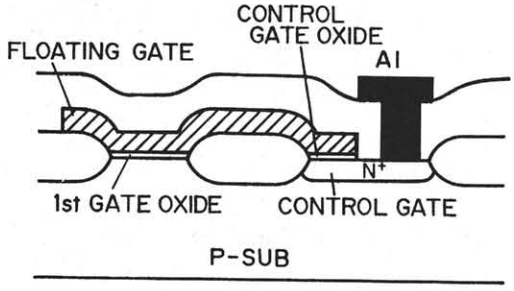

Fig.1. Cross sectional view of single-poly gate EPROM cell(width-direction).

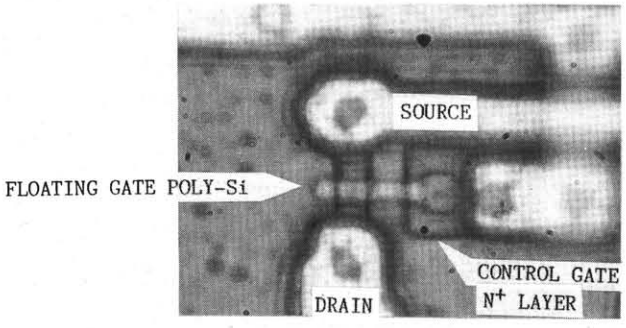

Fig.2. Top view photograph of single poly cell.

Table 1.

L_{eff}	0.7 μm
W	1.2 μm
GATE OXIDE	200 Å
CG OXIDE	200-600 Å
CG N^+	As I/I 2E12 cm^{-2} 100keV
STRUCTURE	As I/I 5E15 cm^{-2}, 35keV
	P I/I 5E15 cm^{-2}, 35keV

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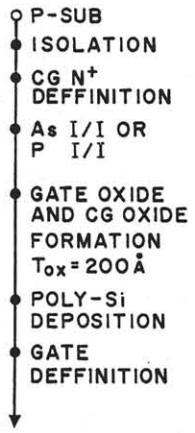

Fig.3. Process sequence for single poly cell.

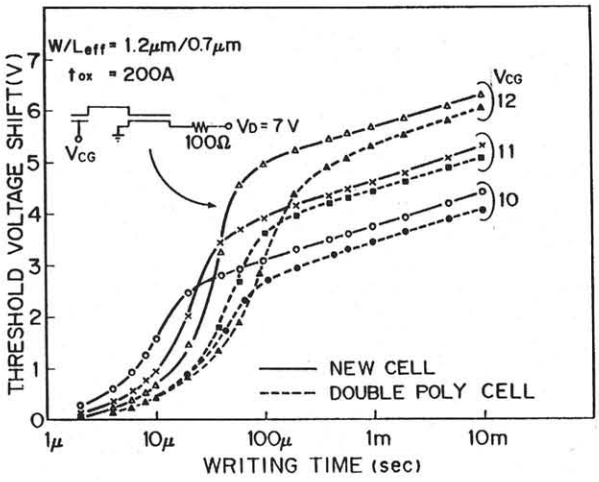

Fig.4. Write characteristics as a function of control gate voltage, V_{CG} compared with that of double poly cell.

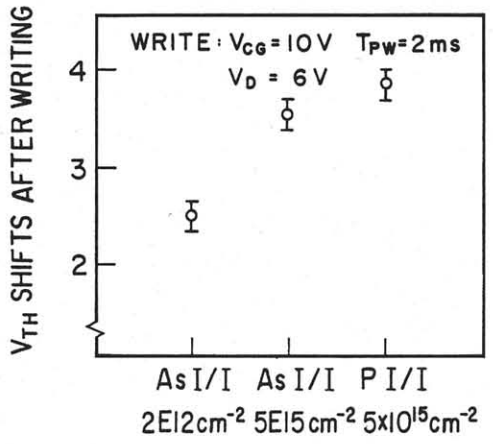

Fig.5. V_{TH} shifts after 2ms writing time as a function of N^+ concentration.

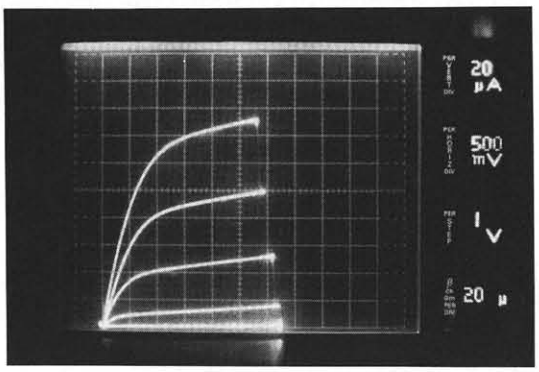

Fig.6. Id-Vd characteristics of single poly cell with 5.5um^2 gate coupling. (L_{eff} = 0.7um, W = 1.2um)

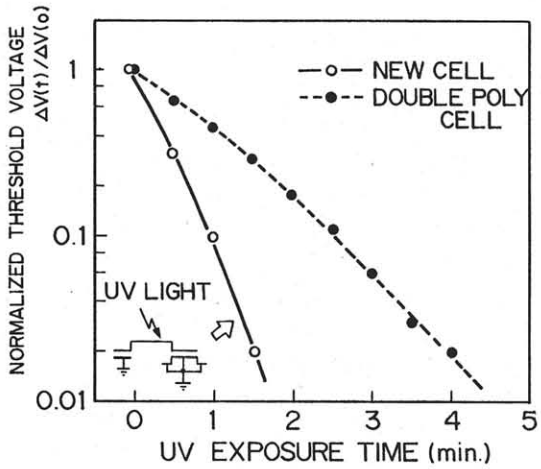

Fig.7. Erase characteristics compared with that of double poly cell.

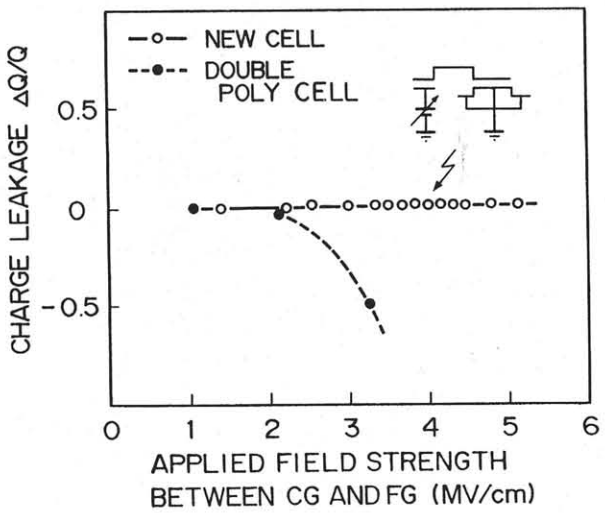

Fig.8. Charge retention characteristics as a function of applied positive gate bias stress.

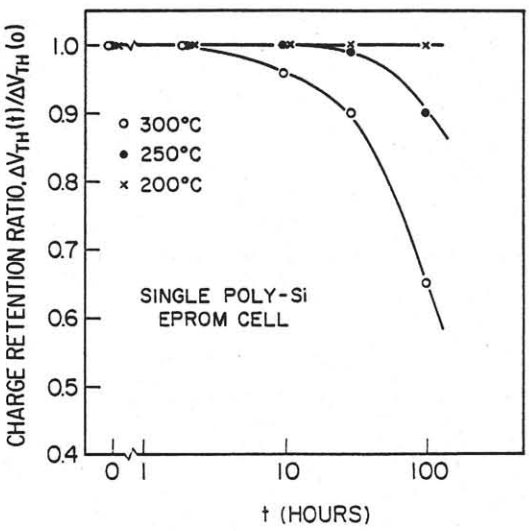

Fig.9. High temperature data retention characteristics of single poly cell.

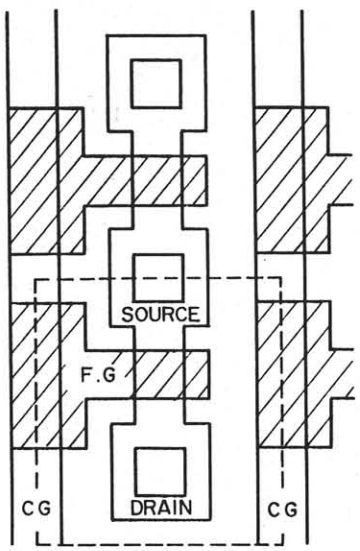

Fig.10. Typical cell layout.