Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 327-330

A Novel EPROM Device Using Focused Boron Ion Beam Implantation

Shoji Shukuri, Yasuo Wada, Takaaki Hagiwara
*Kazuo Komori, and Masao Tamura

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185, Japan
*Musashi Works, Hitachi, Ltd., Kodaira, Tokyo 187, Japan

A novel FAMOS type EPROM device is demonstrated, which has a heavily focused ion beam implanted region at the drain edge of the channel region. This heavily doped region permits higher electric field near the drain edge, resulting in remarkable increase of hot-carrier generation rate, which reduces both the programming voltage and programming time. Three dimensional device simulator, CADDETH, predicted the device characteristics fairly well. Programming time of a fabricated device with effective channel width of 3.1 μm is 50ms, which is 1/50 of that of a conventional device.

1. Introduction

Extensive efforts to accomplish high-density and high-performance EPROM device (Erasable Programmable Read Only Memory) have been demonstrated so far. (1), (2) However, with the increase of memory capacity, programming time per bit should be shortened because of the total programming and testing time. The scaling principle does not improve the programming time because programming voltage is also reduced due to the scaling of the maximum available electric field across oxides to maintain device reliability. Therefore, structural improvement for scaled memory cells primarily aiming for the increase of electric field near the drain edge is necessary to improve programming efficiency.

This paper reports an application of focused ion beam (FIB) doping (3) to high performance device structure as a selective channel doping technique. The simulation results by a three dimensional device simulator are compared with the fabricated device characteristics. Finally, applicability and limitations of FIB-EPROM is discussed.

2. Device Structure and Simulation

2.1 Device Structure

The FAMOS device structure with a FIB doped p^+ region has a self-aligned double-poly Si stacked gate as schematically shown in Fig. 1. The novel feature integrated is a heavily doped p^+ layer formed by FIB B^+ implantation in the middle of the channel. The width of this p^+ layer depends only on the FIB diameter and subsequent thermal processes. The most effective position of the p^+ layer for increasing the electric field and enhancing the hot-electron injection into the floating gate is the drain edge. This structure was chosen only from the device fabrication point of view, because the alignment accuracy almost does not affect the device characteristics.

2.2 Simulation of Device Characteristics

In order to realize high speed programming, electric fields near the drain edge should be high enough to generate enough number of hot-electron which should is injected into the floating gate. The potential and electric field distribution in the channel region of FIB-EPROM device are simulated by the three dimensional device simulator, CADDETH (4). Structural parameters of device simulation are listed in Table. 1.

Figure 2 shows the electric field distribution at the surface of the channel region in the FIB implanted device with a dose of $1\times10^{13}\,cm^{-2}$ under a drain and gate bias of 5V. The result

indicates that the maximum electric field of FIB implanted device is about 6 times higher as compared with that of conventional one. The high electric field should generate 3 orders of magnitude more electron than in the conventional one under the same bias conditions.

3. Experimental Procedures

3. 1 FIB Implantation System

A 100keV focused ion beam implantation system with a Ni-B-Si liquid metal ion source (5) was utilized in device fabrication. Maximum field size on the wafer is 300 μm at an acceleration energy of 100keV. Beam alignment was performed by detecting alignment marks formed by LOCOS edge within the beam field, and the alignment accuracy of the present system was around 0.4 μm. The beam diameter of B^+ FIB was 0.16 μm at 1/e from the peak intensity.

3. 2 Device Fabrication

Figure 3 depicts an optical micrograph of EPROM devices fabricated using FIB channel implantation. These devices were fabricated by a conventional n-channel poly Si-gate technology, on a p-type, (100) oriented, 10 ohm·cm wafer. The gate lengths of the fabricated devices were between 1.5 and 9.5 μm. The gate oxide thickness was 38nm, and poly-Si gate thicknesses were 0.2 μm.

Focused B^+ ion beam was scanned along the channel direction of the MOS devices and was implanted both through the poly-Si floating gate and gate oxide layer with line doses ($L=I_p/e\ v$, I_p;beam current, v;beam scan speed) of between 1.5×10^{8} and $1.5\times10^{11}cm^{-1}$. The accelerating energy was 80keV, and the projected range of B^+ ions locate at the gate oxide and silicon substrate interface. Subsequent thermal processings after FIB implantation were almost equivalent to 1000°C, 60min annealing.

4. Results and Discussions

4. 1 EPROM Device Characteristics

Figure 4 shows the effective channel width (W_{eff}) dependence threshold voltage (V_{th}) of conventional devices before programming, which indicates that the narrow channel effect are found for devices with W_{eff} of less than 3 μm.

The sub-threshold characteristics of the drain current as a function of gate voltage for the conventional and FIB-EPROM devices is shown in Fig. 5. These results indicate that the tailing factors do not change with FIB implantation. On the other hand, the threshold voltage before programming operation increases with increasing the line dose. This increase is attributed to the increase of effective FIB implanted layer width due to the beam tailing as reported in (6).

4. 2 Programming Characteristics

The threshold voltage sift (ΔV_{th}) dependence on programming drain voltage for a 5.1 μm channel width device is shown in Fig. 6. The drain voltage required to shift ΔV_{th} by 3V is reduced to around 9V at a $1.5\times10^{9}cm^{-1}$ line dose. More than a 14V drain voltage is required to obtain the same V_{th} shift for the conventional device. However, FIB doping effect on reducing programming voltage is weakened with narrower the channel width. This phenomenon is mainly attributed to the narrow channel effect due to the increase of impurity concentration in the channel region by side-diffusion of channel stop impurities during field oxidation, as shown in Fig. 4. One possible solution to improve the FIB doping efficiency is trench isolation which reduces the narrow channel effect.

The threshold voltage sift (ΔV_{th}) dependence on programming time is shown in Fig. 6. Programming time of a 3.1 μm channel width device is also reduced by about two orders of magnitude, to about 50ms, as shown in Fig. 7.

4. 3 Cause of Drain Leakage Current

A large drain leakage current is found for FIB implanted one with a line dose of $1.5\times10^{10}cm^{-1}$, as shown in Fig. 5. The cause of leakage current was simulated by CADDETH, to make it clear whether it originate from the structural effect. In the heavily FIB implanted device, large amount of electron and hole pair is generated in the p^+n^+ junction near the drain. A hole current flow in the p^+ layer and an electron current flow down to substrate and cause a drain leakage current.

In addition, the secondary defect should be affected the drain junction characteristics due to the dense radiation damage formation by the high dose rate ion implantation of FIB. (7)

5. Conclusion

A novel EPROM device was fabricated using FIB doping technology on n-channel Si-gate NMOS structure. This device has FAMOS type structure with a selectively heavily doped layer in the channel region formed by FIB implantation. Higher electric field near the drain is realized by the selective heavy channel doping which reduces programming voltage and improves programming speed. However, degradation of MOS device characteristics arose from the beam tailing of FIB profile.

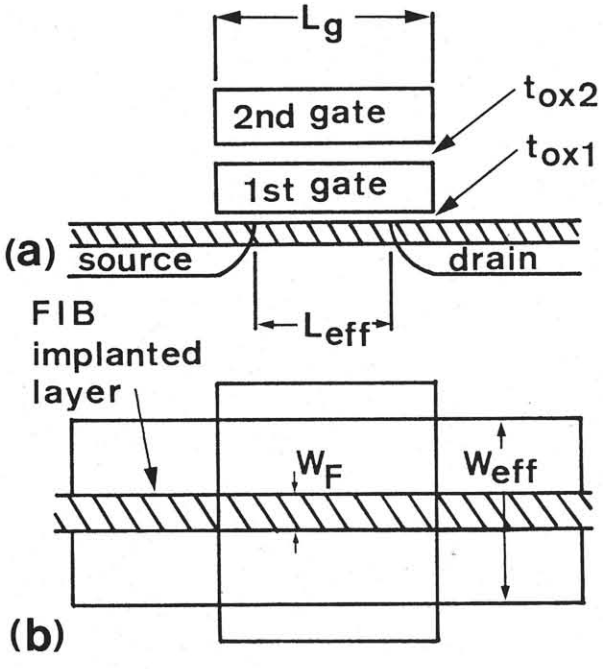

Fig. 1. Schematic cross sectional (a) and top view (b) of fabricated EPROM device.

6. Acknowledgements

The authors would like to express their thanks to Drs. T. Ishitani, H. Tamura, H. Masuda, and Mr. K. Umemura for their fruitful discussions and continuous encouragements throughout the work.

References

1) K. Komori et al. ; IEDM Tech. Dig. (1985)627.
2) Y. Mizutani et al. ; IEDM Tech. Dig. (1985)635.
3) S. Shukuri et al. ; Jpn. J. Appl. Phy. 23 (1983)L543.
4) T. Toyabe et al. ; IEEE Trans. Electron Devices ED-32, (1985)2038.
5) T. Ishitani et al. ; J. Vac. Sci. Technol. 20 (1982)80.
6) S. Shukuri et al. ; J. Electrochm. Soc. to be published.
7) M. Tamura et al. ; Nucl. Instr. and Methods B7/8 (1985)858.

Table. 1 Simulation parameters

Effective channel length	L_{eff}=1.0 μm
Effective channel width	W_{eff}=3.0 μm
Gate oxide thickness	t_{ox}=38nm
Source and drain depth	X_j=0.3 μm
FIB implanted layer width	W_F=0.2 μm
FIB implanted layer depth	X_{jF}=0.5 μm

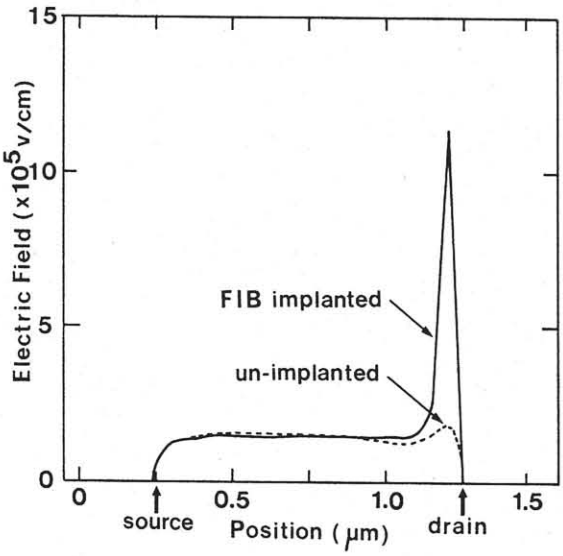

Fig. 2. Electric field distribution in the channel simulated by CADDETH.

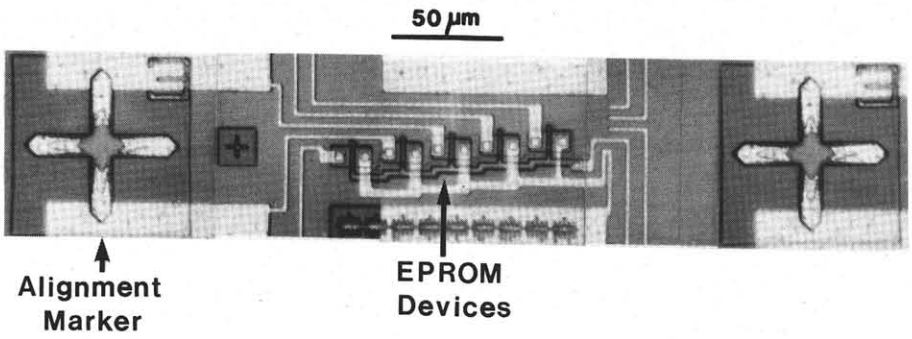

Fig. 3. Optical micrograph of fabricated MOS devices with two 80x80 μm^2 alignment marks on either side

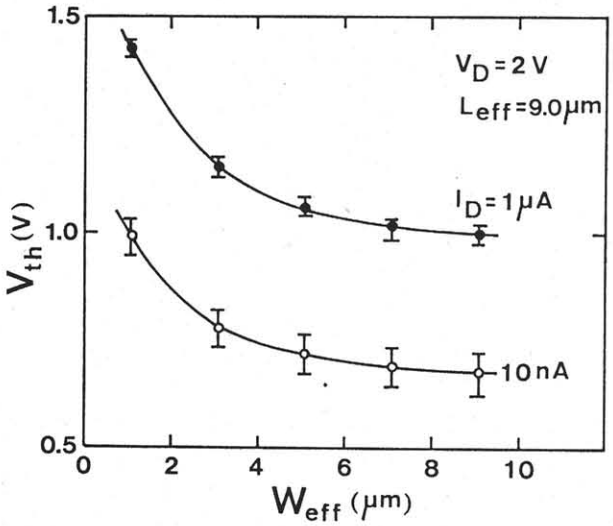

Fig. 4. Relationship between threshold voltage and effective channel width.

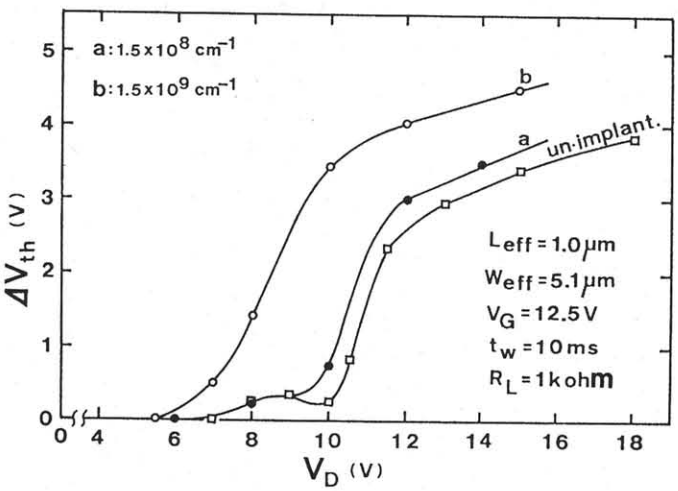

Fig. 6. Programming drain voltage and threshold voltage relationship for the fabricated device with channel width of a 5.1 μm.

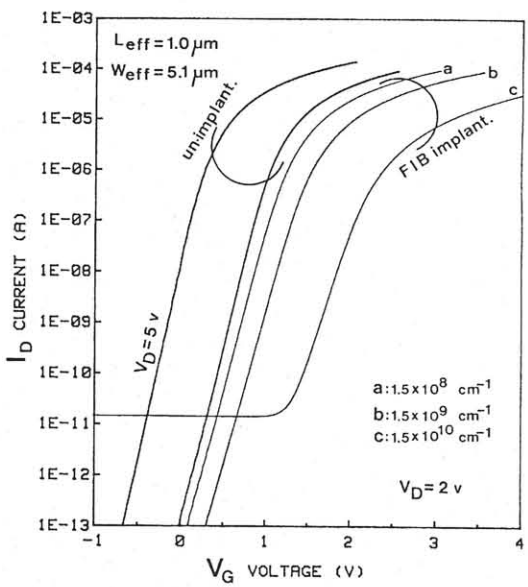

Fig. 5. Gate voltage dependence on drain current for fabricated devices.

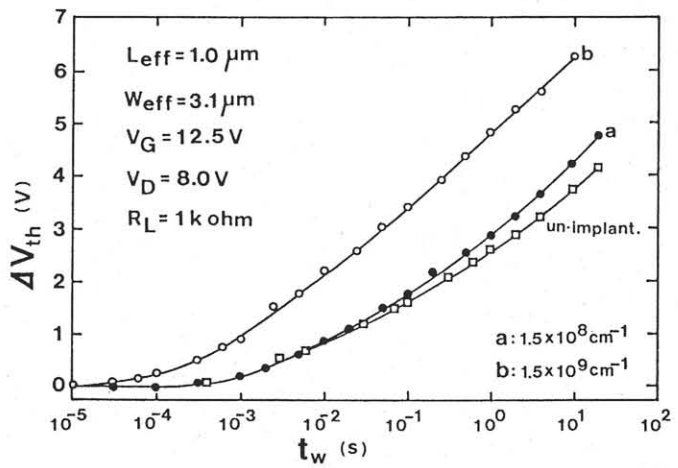

Fig. 7. Programming time and threshold voltage relationship for the fabricated device with channel width of a 3.1 μm.