Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 517-520

Invited

Cross Sectional TEM Obervation of VLSI Devices and Thermal Oxide Morphology

Seiichi ISOMAE and Shigeru AOKI

Central Research Laboratory , Hitachi Ltd.,
Kokubunji , Tokyo 185 , Japan

From the standpoint of spatial resolution, TEM observation of the cross section of a device is indispensable in analyzing problems which occur in the VLSI fabrication process. The present paper describes sample preparation for vertical cross sections in TEM and several device cross sections are shown. The oxide morphology observed in TEM is compared with the simulated results using a new two-dimensional oxidation model.

1. Introduction

As the level of integration in semiconductor devices has increased, ,device dimensions have decreased and device structures have become increasingly complex. Therefore, diagnostic techniques capable of high spatial resolution are needed for solving probelems that arises in the devices fabrication processes. The most suitable tool for this purpose is Transmission Electron Microscopy (TEM). In particular, TEM observation of a device's cross section provides valuable information on device structure [1].

TEM studies on cross sections of thermal oxide reveal that the retardation of oxidation rate occurs in the oxidation of nonplanar silicon surfaces. It is widely accepted that the retardation is related to the stress induced during thermal oxidation [1]-[3]. However, at present, it is difficult to measure this oxidation induced stress using conventional methods. Because of the need to evaluate oxide morphology, an accurate oxidation simulation which includes a stress analysis is needed.

This paper presents several application examples of cross sectional TEM for VLSI structure and thermal oxide morphology. The first section describes the procedure for preparing samples for vertical cross section. Next, TEM photogrphs of the cross sections in the VLSI devices are presented. Finally, simulated results using a new two-dimensional oxidation model which is capable of explainning observed oxide morphology is briefly described.

2. Sample Preparation

Samples for TEM study are prepared as a thin film through which an electron beam can easily pass. Compared with the preparation of horizontal cross sections, the preparation of vertical cross sections (perpendicular to the wafer surface) presents a number of difficulties. One is that careful treatment is required during thinning to protect features. Another problem is the difficulty of including the desired area in the thin-film section..

Figure 1 shows the procedure for preparing cross sections. First, a small piece (about 5 mm square) containing the area of interest is cleaved from the wafer. Several such pieces are stacked like a sandwich and bonded together with epoxy resin. The stacked samples are then lapped to a thickness of about 20 μm with lapping and abrasive powder. After lapping, the thinned samples are set on a small molybdenum holder for the electron microscope. Futhermore, the samples are then thinned to less than 200 nm thick using an ion milling machine. The sample thickness is judged to be sufficiently thin by the transparency of the thinned area and by the milling time. From standpoint of image doubling, the thinner the sample is , the better.

3. Cross sectional TEM photographs

Figure 2 shows a cross sectional TEM photograph of an n-channel MOS memory device with a trench capacitor. Using this figure, it is possible to evaluate the morphology or shape of the patterned features, grain structure and crystal defects near the gate edge.

Enlargements of the gate region and the upper right corner region of the right trench in this device are shown in figures 3 and 4, respectively. In the former, the 20-nm thick gate oxide can be clearly observed. Dislocations can also be observed at a depth of 100 nm. In the latter figure, a three-layer film consisting of $SiO_2/Si_3N_4/SiO_2$ is distinctly visible. This feature can not be seen using any other method.

Figure 5(a) and (b) show an as-implanted sample and one subjected to heat treatment, respectively. In figure 5(a), the black area corresponds to the amorphous layer formed by ion implantation. The fine black lines emanating from the amorphous layer are considered to be dislocations. After heat treatment, the amorphous layer becomes a single crystal including dislocation loops as a result of solid phase epitaxy.

Figure 6 shows a LOCOS structure. In this case, the polysilicon deposited on the oxide surface make it possible to see the very thin oxide film formed by oxidation of the nitride.

Figures 7(a) and (b) show the oxide shape in a nonplanar silicon surface when the surface was oxidized in dry O_2 at 1100°C and 1000°C, respectively. The shape of the upper corners is different. Since the viscosity of the oxide decreases with temperature, the higher the oxidation temperature, the shorter the stress relaxation time. Thus, this difference is primarily due to the difference in the viscoelastic behavior of the oxide.

Figure 8 shows a High Resolution TEM (HRTEM) image at the tip of the upper corner which was oxidized at 1000 °C.

4. Oxidation-induced stress

A new two-dimensional oxidation model based on steady-state oxidant diffusion and viscoelastic deformation of the oxide is introduced to simulate the oxide shape and to analyze oxidation-induced stress. This model takes into account the deformation of silicon in viscoelastic behavior resulting from the volume expansion. As a result, the present model makes it possible to analyze stress induced in silicon, which could not be done in previous models [4]-[7].

Figure 9 shows a simulated profile and stress σ_{yy} for a LOCOS structure. The normal stress σ_{yy} means the stress acting in the y direction on the plane normal to the y axis. Since the positive and negative signs in the normal stress indicate tensile and compressive stress, respectively, it is easily seen that large tensile and compressive stresses are induced near the silicon/oxide interface in the nitride-covered region. In the region where a large stress is induced, the simulated profile differs from the corresponding profile in the TEM photograph [7].

Figures 10(a) and (b) show normal stresses σ_{xx} and σ_{yy} induced during oxidation of the nonplanar surface, respectively. Although there are minor differences compared with observed results, the simulated profile clarifies that oxide retardation arises near the corners. In the upper corner region, a large compressive stress is induced. On the other hand, tensile stress is predominant near the lower corner. This suggests that oxidation in the corner region is retarded by a large stress.

From the above simulated results, it can be concluded that stress is an important factor in explainning oxide retardation. However, many problems remain to be solved before the retardation mechanism can be fully understood.

5. Summary

Cross-sectional TEM observation, as illustrated in the present paper, provides useful information on device morphology and the behavior of crystal defects induced near the silicon surface. The introduction of new process technology and materials in ULSI device fabrication is resulted in a number of problems which remain to be

solved. Consequently, TEM study on cross-sections of the devices will increasingly play a more important role in analyzing these problems. In addition, an accurate two-dimensional oxidation simulation which includes a stress analysis must be developed to evaluate this new process tecnology.

Acknowledgements

The authors wish to thank Mr. S. Yamamoto for his helpful advice on this simulation.

References

1. R. B. Marcus and T. T. Sheng, Transmission Electron Microscopy of Silicon VLSI circuits and Structures, John Wiley & Sons, New York, 1983.
2. K. Yoshikawa, Y. Nagakubo and K. Kanzaki, Proc. 16th Conf. Solid State Device and Materials, p. 475, 1984.
3. D. K. Kao, J. P. McVittie, W. D. Nix and K. C. Saraswat, IEDM Tech. Dig., p. 388, 1985.
4. D. Chin, S. Y. Oh, S. M. Hu, R. W. Dutton and J. L. Moll, IEEE Trans. Electron Devices, vol. ED-30, p. 744, 1983.
5. H. Matsumoto and M. Fukuma, IEEE Trans. Electron Devices, vol. ED-32, p. 132, 1985.
6. T. L. Tung and D. A. Antoniadis, IEEE Trans. Electron Devices, vol. ED-32, p. 1954, 1985.
7. S. Isomae, S. Yamamoto, S. Aoki and Y. Yajima, to be published in IEEE Electron Devices Lett., vol. EDL-7, 1986.

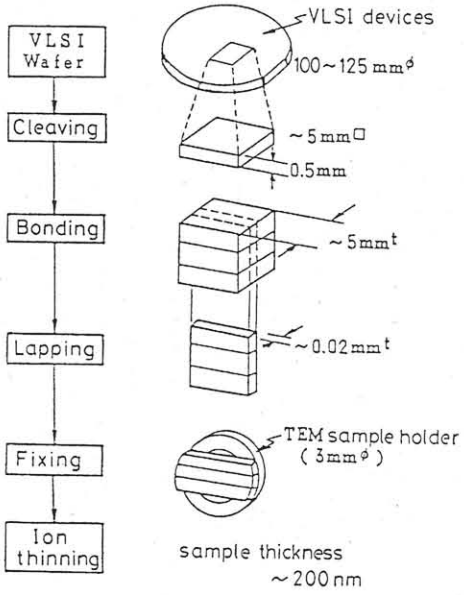

Fig. 1 Sample preparation for cross sectional TEM.

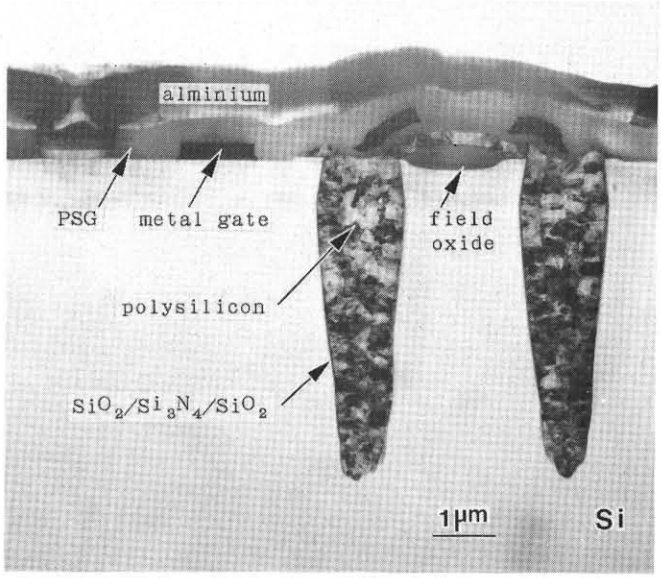

Fig. 2 Cross sectional TEM photograph of a trench capacitor DRAM cell.

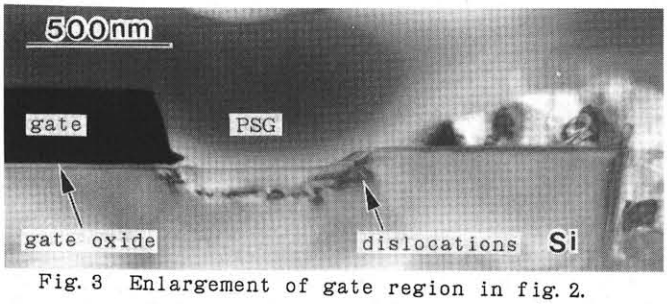

Fig. 3 Enlargement of gate region in fig. 2.

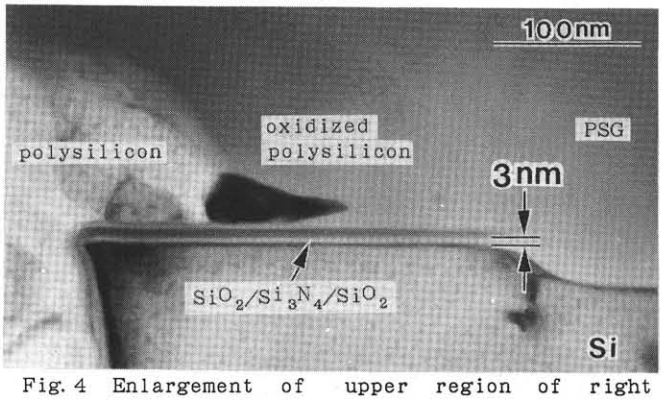

Fig. 4 Enlargement of upper region of right trench in fig. 2.

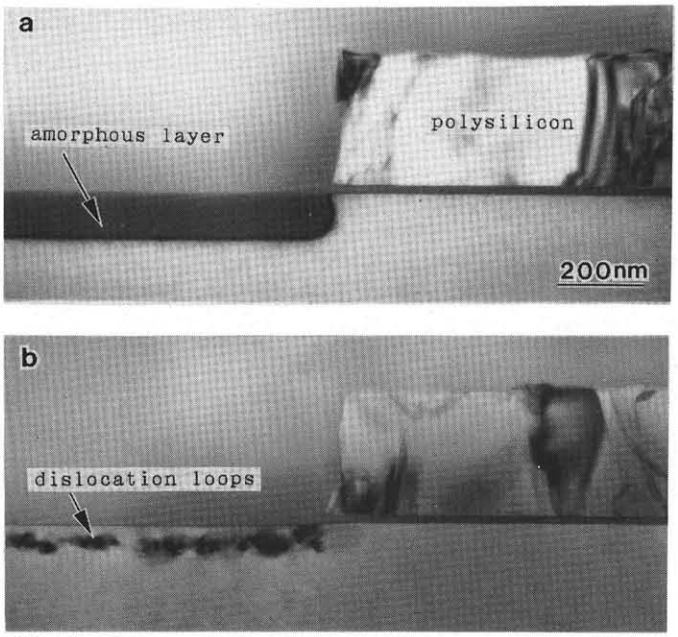

Fig. 5 Cross sectional TEM photograph of As ion ($5x10^{15}$ cm^{-2} at 80 Kev) implanted region.
(a) before annealing.
(b) after 10 min annealing in N_2 at 950 °C.

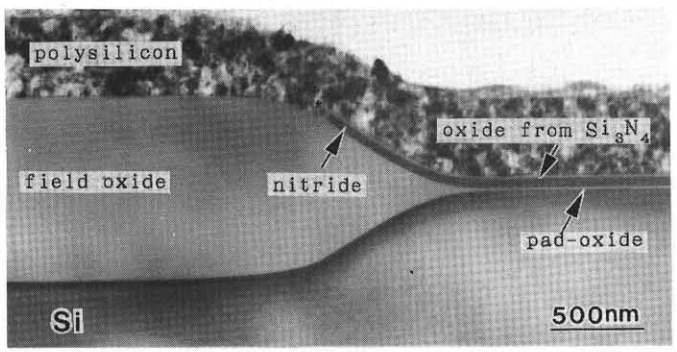

Fig. 6 Cross sectional TEM photograph of LOCOS structure (50nm Si_3N_4/20nm pad-SiO_2) after 5hr wet oxidation at 1000 °C.

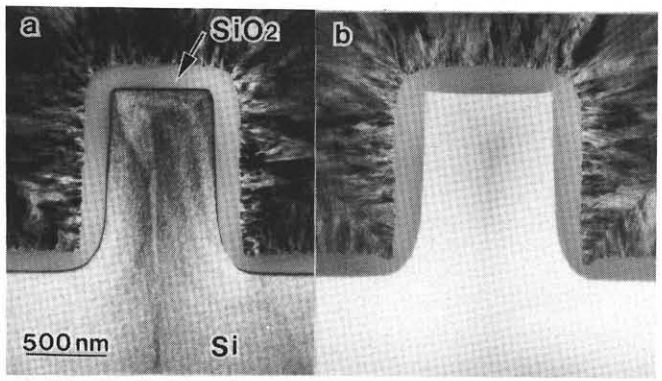

Fig. 7 Oxide shape in thermal oxidation of a groove.
(a) 1100 °C, 1.5 hr. (b) 1000 °C, 5 hr.

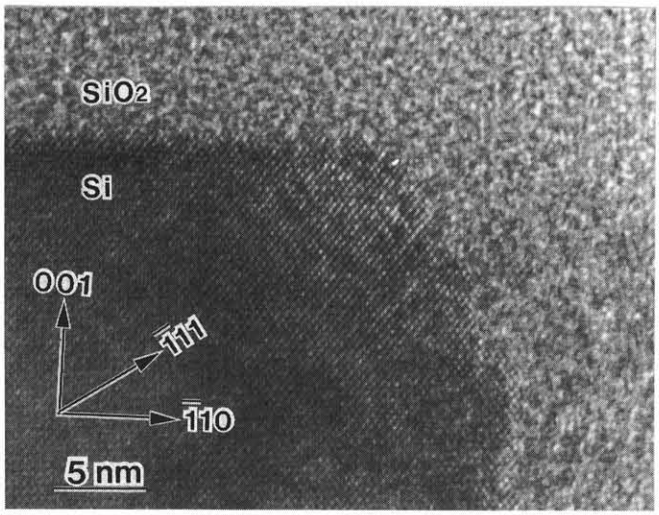

Fig. 8 HRTEM image at upper corner region of groove.

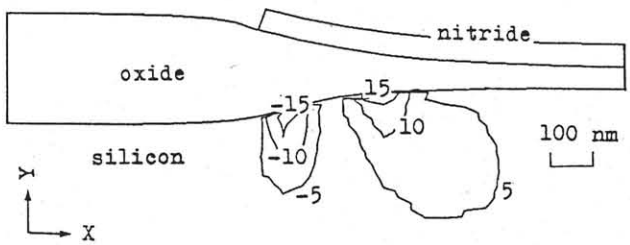

Fig. 9 Simulated oxide profile and stress σ_{yy} distribution in a LOCOS (50nm Si_3N_4/50nm SiO_2) after 30 min wet oxidation at 1000 °C. Stress units are MPa.

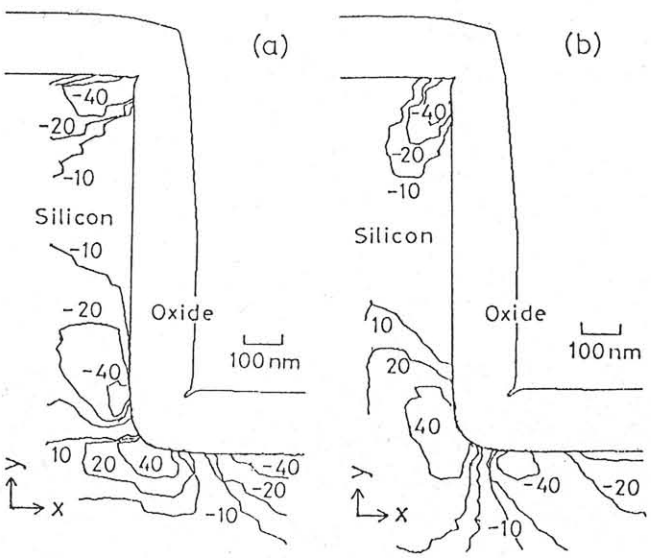

Fig. 10 Simulated oxide profile in thermal oxidation (1000 °C, wet, 15 min) of nonplanar surface. Stress units are MPa.
(a) stress σ_{xx}.
(b) stress σ_{yy}.