Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 533-536

Lattice Configuration and Electrical Properties at the Interface of Direct Bonded Silicon

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A new direct silicon bonding method has been developed. TEM observation showed that epitaxial-like lattice continuity was formed at the bonded interface when the orientations of bonded surfaces were adjusted, and that an amorphous layer was formed when the orientations changed. However, the electrical resistance of the bonded interface was less than $10^{-6}\Omega cm^2$, regardless of bonded surface orientations. A diode including an amorphous layer at the bonded interface showed good current voltage characteristic.

1. Introduction

A silicon to silicon direct bonding method (SDB) has been developed[1]. A pair of mirror polished wafer surfaces, which have been cleaned and hydrophilized, can adhere tightly at room temperature; when they are brought into contact. Subsequent heating increases bonding strength until it reaches the bulk silicon value. Oxidized surfaces also can be bonded by SDB.

The SDB mechanism is considered to be as follows. Silanol (Si-OH) groups have been formed on the hydrophilized wafer surfaces. The adhesion at room temperature takes place as the result of interaction between the silanol groups. At an elevated temperature, dehydration condensation reaction occurs to form Si-O-Si bonds. As the heating continues, Si-Si bonds replace Si-O-Si bonds and oxygen atoms diffuse into bulk silicon. Finally, the silicon atoms in both wafers bond directly.

The wafers bond tightly, not only mechanically but also electrically. These bonded wafers can stand severe thermal and chemical treatment during device fabrication, because no bonding material is used. Therefore, SDB is very useful for various kinds of device fabrications. Preferable SDB applications, on the basis of merit, will be:

a) Replacing the impurity diffusion by bonding different impurity type or different concentration wafers. A deep and steep impurity change is obtained in shorter time.

b) Replacing epitaxial growth. A thick layer with low impurity concentration is formed without autodoping.

c) Making SOI wafers by bonding oxidized wafers. A defectfree single crystalline layer on an insulator is obtained.

d) Machining in silicon bodies by bonding grooved or holed surfaces. This method is useful for sensor devices.

Using the SDB, a silicon wafer surface can be directly bonded, even to a different orientation surface. However, because of the lattice mismatch, the state of the bonded interface would change, according to the lattice orientations of the two bonded surfaces. Therefore the lattice configulation and the electrical properties at the interface were investigated in relation to lattice orientations of the bonded wafer surfaces. This paper reports the results.

2. Experiments

Commercially available mirror polished wafers were used in these experiments. The flatness and roughness were similar to that utilized in integrated circuits.

The wafers were cleaned by inorganic acid solutions and rinsed by deionized water. The wafer surfaces were hydrophilized during these treatments. After they were dried, a pair of the wafer surfaces were placed together in a clean air atmosphere, so that they would adhere. This contact formed self-adherence throughout the surface. At that time, the orientation flats of paired wafers were fitted to each other. However, in some pairs, one wafer was rotated to about 45 or 90 degrees off, versus the other wafer. Adhering a (100) wafer to a (111) wafer was also carried out. The combinations of the bonded surface orientations and used wafers were summarized in Table 1.

Self-adhering wafer pairs were heated at 1000°C for 1 hour in a nitrogen ambient. No weight was applied on the wafers during heating. The wafers were completely bonded.

Lattice configurations at the bonded interfaces were observed by high resolution transmission electron microscope (TEM). The equipment used was JEOL JEM-2000EX. The Cross sections of pieces cut from samples 1 to 3 were mechanically ground and then ion milled for this observation.

Table 1. Used wafer characteristics and combinations of bonded wafers.

Wafer characteristics	
N(100); n-type(100) ρ= 1.5 Ωcm P(111); p-type(111) ρ= 0.002Ωcm P(100); p-type(100) ρ= 0.002Ωcm	
Sample No.	Combinations
1	N(100)/N(100) 0°
2	N(100)/N(100) 45°
3	N(100)/P(111) 45°
4	P(100)/P(100) 0°
5	P(100)/P(100) 45°
6	P(111)/P(111) 0°
7	P(111)/P(111) 90°
8	P(111)/P(100) 0°

The electrical resistance for the interface was measured, using chips made from bonded wafers. On the n-type surfaces, heavily doped n^+-layers were formed in order of ohmic contact. Aluminum electrodes were evaporated on both surfaces of the wafers. Then the wafers were cut into 3mm square chips. Current voltage (I-V) characteristics for the chips were measured by the four-probe method at room temperature. Potential profiles were obtained using a needle probe on the side surface of the chips under an electric current.

Sample 3 has a p-n diode structure. The n-type wafer side was ground down to 30μm. After an n^+-layer was formed on the ground down surface, aluminum electrodes were evaporated on both wafer surfaces. Diode chips were cut from the metallized wafer.

3 Results and discussion

Figures 1 to 3 show TEM lattice image photographs at cross-sectional bonded interfaces. When two (100) surfaces are bonded in fitting the orientation flats for both wafers, the lattice arrangement continues beyond the bonded interface, as is shown in Fig. 1. According to the electron beam diffraction, the angle between lattice orientation for both wafers is below 0.5 degree. The interface seems to have been formed by epitaxial growth. However at lower magnification, few cluster of lattice defects were observed at some part of the bonded interface, and several dislocations extended to distant areas from the interface. On the other hand, lattice defects were concentrated at the interface, when one wafer was rotated versus the other (Fig. 2). In this photograph, no lattice image can be obserbed clearly on one side of the interface, because the angle between the wafers is not exactly 45 degrees. Electron beam diffraction shows it is about 40 degrees. These results suggest that re-arrangement of silicon atoms

occurs during heat treatment, and that the mismatch at the bonded interface is compensated for by the re-arrangement, if the mismatch is small. When (100) and (111) surfaces are bonded, a 3nm thick amorphous layer is formed, as is shown in Fig. 3. This layer would compensate for the great lattice mismatch between two different surfaces. The lattice defect, neighbouring on the interface, is scarcely observed.

The I-V characteristics for the bonded wafers (sample 4 to 8) were ohmic, from 0.22 to 110A/cm² in current density at room temperature. The measured electrical resistances for chips agreed with the calculated values in which no resistance at the bonded interface was assumed. Similar ohmic relationships were obtained for samples 2 and 3. Figure 4 shows the surface potential profile for sample 7 under a 22A/cm² current flow. No potential gap is observed. The same results were obtained for samples 4 to 8. Therefore it can be concluded that the interface resistance is below the experimental error ($10^{-6}\Omega cm^2$).

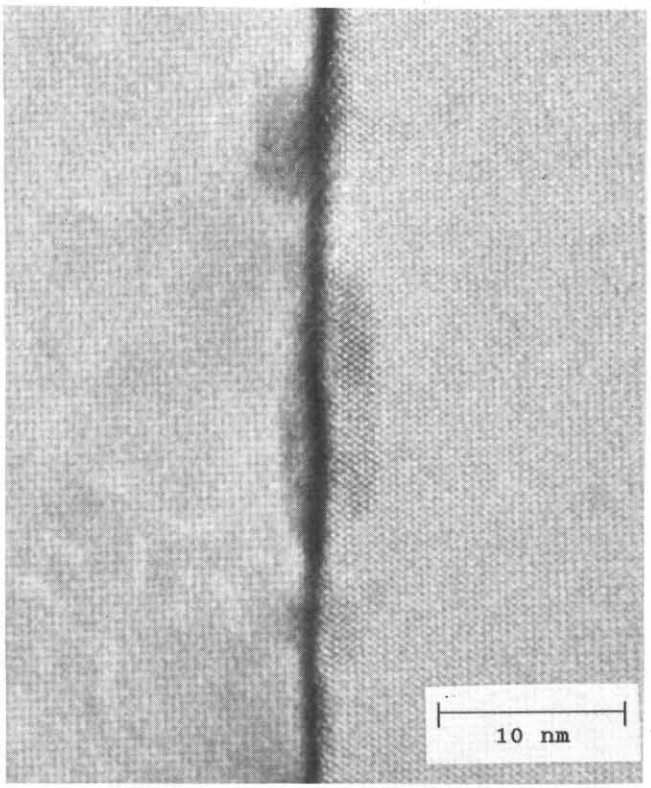

Fig. 2 TEM lattice image at cross-sectional bonded interface for sample 2.

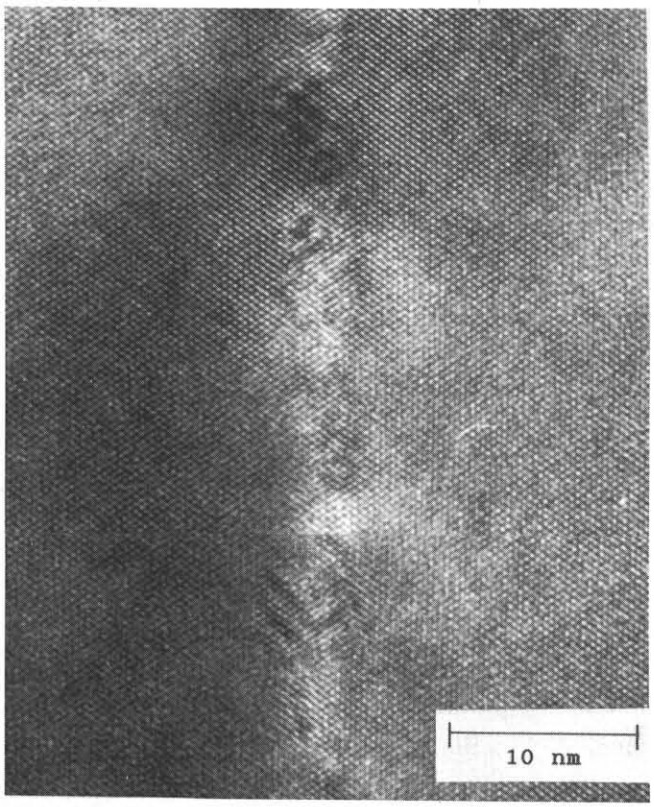

Fig. 1 TEM lattice image at cross-sectional bonded interface for sample 1.

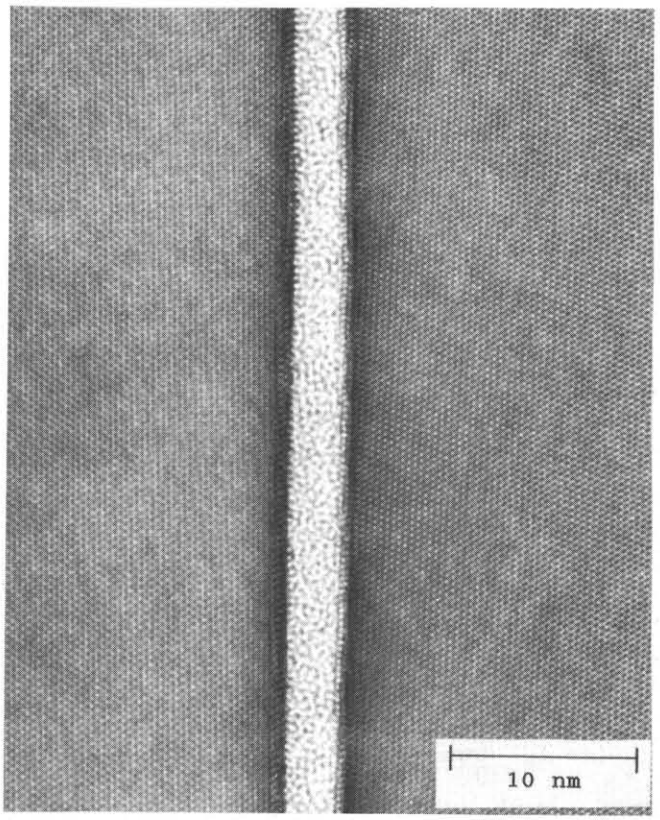

Fig. 3 TEM lattice image at cross-sectional bonded interface for sample 3.

The I-V characteristics for sample 3 diode were measured. Figure 5 shows forward characteristics of the 2mm square chip. The amorphous layer at the bonded interface does not seem to cause the voltage drop. The value of n in the equation;

$$I=Aexp(qV/nkT)$$

where A is constant, q is an electron charge and k is Boltzmann constant; is 1.10. Figure 6 shows backward characteristics for a mesa cut 8mm diameter diode. Breakdown occurs at 60V. The impurity diffusion during the heat treatment mooved the p-n junction toward the n-type wafer direction. Therefore, backward characteristics are not considered to be affected by the interface, which is positioned in the high impurity p-layer. A 1800V breakdown diode was fabricated by directly bonding a p-type wafer to a lower impurity concentration n-type wafer in the former work[1].

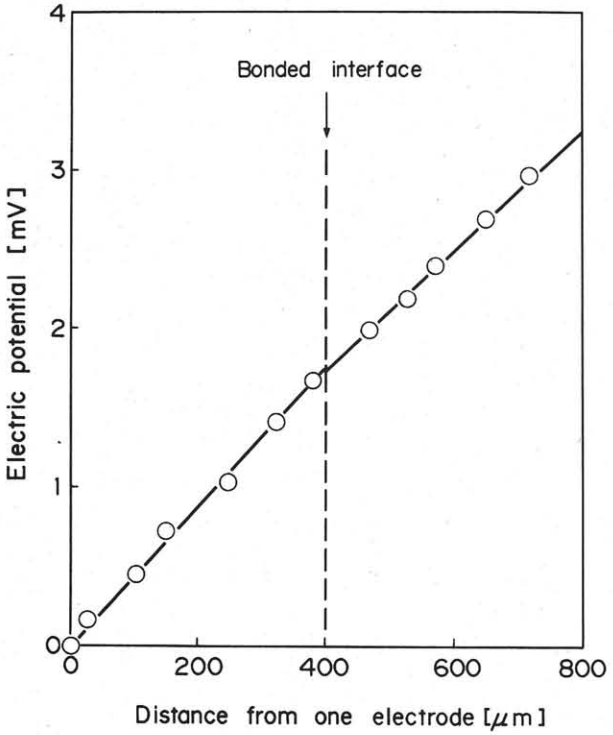

Fig. 4 Potential profile on the side surface of the 3mm square sample 7 chip at 2A current.

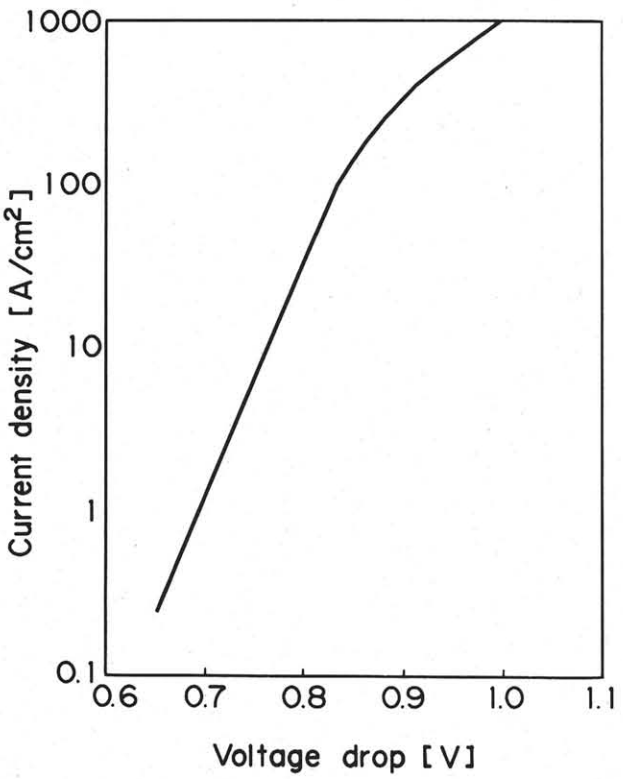

Fig. 5 Forward I-V characteristics for sample 3 diode chip.

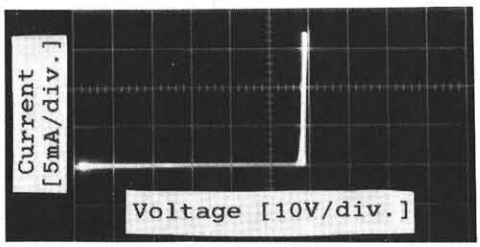

Fig. 6 Backward I-V characteristics for sample 3 diode chip.

4. Summary

Silicon wafers were bonded by SDB. The combinations of bonded wafer surfaces were varied. TEM observation showed that the interface is epitaxial-like, when the orientations of bonded surfaces are adjusted and that the interface is amorphous when different orientation surfaces are bonded. The electrical resistance for the interface is less than $10^{-6}\Omega cm^2$ for all combinations examined. A diode of good I-V characteristic was fabricated by SDB.

5. Acknowledgment

The authors would like to thank K. Shibata of JEOL for TEM photographs.

6. Reference

1) M. Shimbo, K. Furukawa, K. Fukuda, K. Tanzawa, Ext. Abs. 169th Electrochem. Soc. Meating, pp. 337 (1986)