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III-V Semiconductors on Si Substrates

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Recent advances in lattice mismatched epitaxial technology has allowed the demonstration of GaAs based devices on Si substrates with performance nearly identical to their counterparts on GaAs substrates. The advantages of using Si as a substrate (higher thermal conductivity, larger size and higher mechanical strength) will lower the cost of GaAs IC production. Monolithic integration of Si based and GaAs based devices is also an attractive possibility. One micron gate GaAs MESFETs on Si with transconductances of $g_m = 180 \text{ mS/mm}$, and current gain cutoff frequencies of $f_T = 13 \text{ GHz}$ have been obtained. These values are comparable to similar geometry state-of-the-art GaAs MESFETs on GaAs substrates. Heterojunction bipolar transistors (HBTs) with $f_T = 30 \text{ GHz}$ and $f_{max} = 11 \text{ GHz}$ for $4 \times 20 \mu \text{m}^2$ emitters have been obtained on Si. These compare favorably with the highest reported values for HBTs on GaAs. Common emitter current gains of $\beta = 13$ were obtained, which is not limited by recombination in the neutral base region.

§1. Introduction

The potential benefits of GaAs growth on Si substrates has precipitated a recent surge of activity in this area.¹⁾⁻⁴⁾ The use of Si as a substrate for GaAs epitaxy would allow larger diameter, better thermal conductivity and better mechanical strength. It would also be possible to monolithically integrate⁵⁾ GaAs devices and Si devices taking advantage of the speed of GaAs and the mature processing technology for Si. Optical signals could be generated in such a monolithic system, making optical off chip communication possible.

There are two main difficulties associated with growth of GaAs on Si. The first is that of lattice mismatch -- GaAs has a 4% larger lattice constant than that of Si. This large mismatch will unavoidably cause misfit dislocations. Approximately a misfit dislocation density of 10^{12} cm² is required at the substrate-epi interface to accommodate the mismatch. Inevitably, a certain fraction of these will become sources for threading dislocations. Techniques which confine the dislocation lines to the bottom of the epitaxial structure are required.

The second difficulty is the problem of antiphase disorder. The zincblende lattice is composed of two interpenetrating FCC sublattices, one for the cation and one for the anion. Since Si is a nonpolar semiconductor (i.e., there is no distinction between sublattices), uniform ordering of the polar semiconductor sublattices is not ensured. Upon crossing an antiphase boundary, the sublattices are interchanged. Again growth techniques to suppress this type of defect are needed. In this paper, several growth techniques whereby these problems can be avoided will be outlined. Devices results will also be presented to substantiate their effectiveness.

§2. Materials investigation

Although the exact electrical nature of antiphase disorder is not well understood, it would be preferable to eliminate it. At an antiphase boundary, Ga-Ga and/or As-As bonds occur. The result is that locally there must be an excess positive or negative charge. The excess charge would be a scattering center which would lower mobility. It is unclear whether deep levels would result.

Fortunately, the technique of depositing prelayers is effective in suppressing antiphase disorder. Prelayer deposition is where a (100) oriented substrate is exposed to either a Ga beam or As beam immediately prior to growth. By ensuring uniform coverage of either cation or anion on an atomically flat surface, antiphase domains will not form. This is because in the (100) direction, planes alternate between Ga and As.

In the presence of single atomic layer (or odd numbers of atomic layers) steps, the situation is modified. An antiphase boundary will result at such a step with uniform prelayer coverage. These steps are known to exist in nominally (100) oriented Si.⁶ Several techniques have been used to detect antiphase disorder. These include plan view transmission electron microscopy (TEM), X-ray scattering,⁷ and anisotropic chemical etching.⁸ We have not seen evidence for antiphase disorder by any of these techniques.

Most chemical etches for GaAs attack the {111}B face more rapidly than the {111}A. The {111}A face therefore tends to determine the sidewall shape of a mesa. Upon crossing an antiphase boundary, the {111}A and {111}B faces become interchanged, and antiphase disorder can easily be detected by noting the sidewall shapes. Shown in Figure 1 are scanning electron micrographs of mesas etched in GaAs on Si using an As prelayer (a) and a Ga prelayer (c). Shown in Figure 1(b) is a sample where antiphase disorder was intentionally generated to demonstrate that this technique can reveal antiphase disorder.

The etching technique will probably reveal antiphase disorder if the domain sizes are larger than about 0.2 μ m. To detect antiphase domains of smaller size, X-ray scattering was used. The details of this technique are published elsewhere.⁷⁾ Since no antiphase disorder was detected by any technique even in samples grown on nominal (100) oriented Si, there must be some mechanism whereby antiphase boundaries "heal" or are overgrown.

In order to reduce dislocation densities, several techniques for confining them to the lower part of the epitaxial structure were developed and employed. The first of these techniques is the use of tilted substrate orientations. High resolution transmission electron microscopy (TEM) images⁹⁾ have shown that when a tilted orientation is used, dislocations with their Burgers vectors parallel to the substrate-epi interface are preferentially generated. In contrast, when non tilted (100) orientations are used there are more dislocation with Burgers vectors inclined with respect to the interface. Since it is only the projection of the Burgers vector onto the interface



1 µm



2µm

Fig. 1. Sidewall shapes of GaAs epitaxial layers on Si (100), with an As prelayer (a), antiphase domains (b) and a Ga prelayer (c).

that accommodates mismatch. dislocation with inclined Burgers vectors are less efficient at taking up mismatch. It is not only that fewer dislocations with Burgers vectors parallel to the interface are required, but also that this type of dislocation does not act as a source for threading dislocations.

The role of tilted substrates is to generate the proper type of dislocations such that they do not propagate up through the epitaxial overlayers. If a tilt towards the <011>azimuth is used, steps only occur in one direction. In contrast, if a tilt in a mixed direction, toward the <001> azimuth, is used two dimensional steps occur. In a substrate with two dimensional steps, dislocations are controlled in both directions so that low dislocation densities result.

It is inevitable that at least a small fraction of the dislocations at the interface will be sources for threading dislocations. Since such large misfit dislocation densities are required at the interface, these will result in an unacceptably large dislocation density in the overlayers. We have therefore used GaAs/InGaAs pseudomorphic superlattices as dislocation barriers. The use of these barriers was predicted in principle by Matthews and Blakeslee.¹⁰⁾ As can be seen in Figure 2, very low densities of misfit dislocations at the top of $\sim 2 \,\mu m$ thick films have been obtained using these techniques.



Fig. 2. TEM of a GaAs on Si epitaxial layer showing the very low misfit dislocation densities.

§3. Device Characterization

Many authors have demonstrated high quality GaAs based devices on Si substrates ¹⁻⁴⁾. For GaAs metal semiconductor field effect transistors (MESFETs) on Si, performance comparable to state-of-the-art devices on GaAs substrates has been obtained. Transconductances of 180 mS/mm for 1.2 μ m gate devices on Si have been demonstrated.

It is not only the dc performance that is comparable, but the performance at microwave frequencies. Figure 3 shows short circuit current gain and maximum available gain as a function of frequency for 1.2 μ m gate GaAs MESFETs on Si. As can be seen, a current gain cutoff frequency of $f_T = 13$ GHz and a maximum oscillation frequency of $f_{max} = 30$ GHz. These values compare very well with what has been obtained in comparable geometry transistors on GaAs using both epitaxial and direct implant technology. Equivalent circuit modeling has shown that there is essentially no difference between the devices on GaAs or Si. All element values are almost identical between GaAs on Si and GaAs on GaAs.

Modulation doped field effect transistors (MODFETs) on Si have also been demonstrated. In GaAs/AlGaAs MODFETs on Si, transconductances for 1 μ m gate devices of 170 mS/mm and 275 mS/mm at 300 K and 77 K, respectively have been reported. As in the case of MESFETs on Si, the microwave performance was nearly identical their counterpart on GaAs. Current gain cutoff frequencies of f_T = 15 GHz and maximum oscillation frequencies of f_{max} = 25 GHz were obtained. It is not only in majority carrier devices that excellent results have been obtained. In minority carrier devices, very encouraging results have also been demonstrated. Heterojunction bipolar transistors (HBTs) on Si have been reported with good perfor-



Fig. 3. Short circuit current gain and maximum available gain plotted versus frequency for a 1.2 μm gate GaAs MES-FET grown on Si.

mance at dc and excellent performance at microwave frequencies.

Shown in Figure 4 is an output current-voltage characteristic of GaAs/AlGaAs HBT grown on Si. As can be seen, a common emitter current gain of $\beta = 13$ is obtained in this devices, with a 0.2 μ m thick base doped to p = 5 x 10¹⁸ cm⁻³. Reduction of defect assisted space charge recombination and surface leakage component of the base current can lead to larger current gains. The offset voltage in these devices is about 0.2 V, which is expected from the difference in turn on voltage between the heterojunction emitter and the homojunction collector.



Fig. 4. Output I-V characteristics of an HBT grown on Si.

Although the current gains in the HBTs grown on Si are high enough for some applications, they are not as high as would be expected from devices with identical structures grown on GaAs. To investigate the mechanism behind this lower gain, we fabricated a series of HBTs with varying base thickness. As mentioned earlier, defects in the material can lower the minority carrier lifetime resulting in a lower base transport factor. If this were the case, then the gain should increase substantially by reducing the base thickness. However, the gain does not improve upon reducing base thickness as gains of $\beta = 13$, 12, and 13 were obtained in structures with $W_B = 0.2$, 0.15, and 0.1 μ m, respectively. This indicates that the gain in these devices is not limited by recombination in the neutral base region. Further studies are in progress to determine the mechanisms which limit the current gain.

Maximum current densities of $160,000 \text{ A/cm}^2$ were obtained in the HBTs on Si without device failure. Upon operating these devices at current densities above 100 kA/cm^2 for several hours, the current gain did somewhat degrade. However, upon operation for several hours at current densities below about 30 kA/cm^2 , no device degradation was observed.

In order to test the high speed performance of these devices, microwave S-parameter measurements were made in the frequency range from 2-18 GHz. For devices with relatively large geometries($4 \times 20 \ \mu m^2$) f_{max} values of 11 GHz were obtained with f_T at about 30 GHz at a current density of 15 kA/cm². With smaller geometries and optimized structures these figures are expected to improve significantly.

§4. Conclusions

 In conclusion, growth techniques for GaAs on Si have been developed. It was shown that these techniques are very effective in reducing dislocation densities and eliminating antiphase domains.

Application of these techniques to GaAs devices has resulted in the achievement of state-of-the-art performance. GaAs MESFETs (1.2 μ m gate) on Si with transconductances of g_m = 180 mS/mm. current gain cutoff frequencies of f_T = 13 GHz and maximum oscillation frequencies of f_{max} = 30 GHz have been obtained. In HBTs, common emitter current gains of β = 13 were achieved. Values for f_T of 30 GHz and for f_{max} of 11 GHz were also obtained for a 4 x 20 μ m² emitter geometry. These results are very encouraging and show the potential for GaAs growth on Si.

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