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Initial Stage of Molecular Beam Epitaxial Growth of GaAs on (100) Si

H. TAKASUGI, T. UEDA and M. KAWABE
Institute of Materials Science, University of Tsukuba
Sakura-mura, Ibaraki 305, Japan
Y. BANDO
National Institute for Research in Inorganic Materials
Sakura-mura, Ibaraki 305, Japan

The initial stage of GaAs growth has been studied by RHEED, AES and HRTEM. The tilting orientation of (100) Si toward <011> is necessary for single domain GaAs. The clean Si surface is easily coverd with one monolayer of As, and the As layer is stable up to about 700 °C. The surface undulation at the initial stage of epitaxy strongly depends on the growth temperature. Several lattice dislocations originating from the difference of lattice constants and contaminants were observed at the interface by HRTEM.

1. Introduction

Recently, there has been an increase in interest in the growth of GaAs on Si. This heterostructure has great potential for device applications. However , there are many problems such as the large differences with respect to electronic polarity, thermal-expansion coefficient and lattice constants. The difference in polarity and lattice constants create antiphase domains and lattice defects, respectively.

Up to now, growth of the first thin buffer layer on Si at low temperature is found to be successful to get device quality GaAs film.[1] Field-effect transistors[2-4], solar-cells[5] and laser-diodes[6,7] have been grown by molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) using Si substrate. However, many questions concerning to the crystal growth, especially in its initial stages, remain unanswered. Observations of initial stages of GaAs growth will be helpful to understand the defect generation mechanism.

In this paper, we firstly studied about the growing feature of the first epitaxial GaAs layer on Si by molecular beam epitaxy (MBE) and secondly the effect of the growth temperature of the first buffer layer on the quality of the epitaxial layer. In order to investigate the growth mechanism, we employed reflection high energy electron diffraction (RHEED), auger electron spectroscopy (AES) and high resolution transmission electron microscopy (HRTEM). The surface undulation of GaAs at several growth temperatures and the defect generation mechanism at the initial growth stages are also reported.

2. Experimental

The MBE system used was ANELVA 830 with an analysis and a preparation chamber. The substrate used was (100) Si oriented 4°±1° off toward the <011>. It was degreased and ecthed with hot-HNO_3 and HF before being mounted onto the substrate-holder block with In. Then, the sample was prebaked at about 300 °C for 1 hr to remove H_2O and other gases and was transferred to the growth chamber.

Prior to the growth of GaAs, the Si substrate was heated up to a temperature of 850 °C to remove oxide layer on the Si surface and to produce biatomic layer surface steps. At first, the GaAs layer was grown at a rate of 100 nm/hr at substrate temperatures of 550, 350 and 80 °C. The growth mode of GaAs was investigated by the auger intensity of Si (=92eV) and As (=1229eV) at various thicknesses of GaAs in the analysis chamber with a background pressure of 1×10^{-9} Torr. RHEED was used to investigate the reconstructed structure of As-covered Si surfaces in addition to the morphology at various stages of GaAs growth. The GaAs/Si interface was examined by

the JEM-4000EX and JEM-200CX, operating at 400 and 200 kV, respectively. Cross-sectional samples for TEM observation, were prepared by thinning with Ar sputtering. The cross-sectional specimen was thinned parallel to (110) plane.

3. Results and Discussions

3-1 RHEED observation

At first, we studied the RHEED pattern from the 4° off Si surface. After the sample was baked at above 850 °C in a growth chamber, it was exposed to As flux. At this stage, the Si surface was covered with a monolayer As. Figure 1 shows the RHEED pattern from the As-covered Si surface, (a) and (b) are <011> and <0$\bar{1}$1> azimuths, respectively. There is a clear difference between the two azimuths, that is, for <011> there is 2x structure and for <0$\bar{1}$1> there is 1x structure. These patterns suggest that the surface step is biatomic layer height. For the growth of single domain GaAs, it is important to obtain a clear 2x1 RHEED pattern from As-covered Si surface. Uhrberg et al. suggested from the theoretical calculation that the symmetric arsenic dimers is likely to be formed on Si (100) surface[8]. If the arsenics on Si surface form dimers, the reconstructed structures from the Si surface without As will be 1x structure for <011> and 2x structure for <0$\bar{1}$1>, and this indicates that the dangling-bond of Si surface align across the terrace. Kaplan pointed out in his studies using LEED that the steps of a biatomic layer height could be obserbed at the vicinal Si (100) surface and the dangling-bond of its surface aligned along the terrace since they were energetically stabler than the one atomic layer steps.[9] We can not explain the two results at the moment.

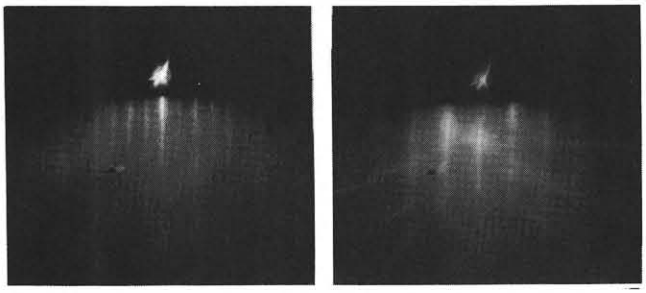

Fig.1(a) Fig.1(b)

Fig.1. RHEED patterns for Si surface. (a) <011>, (b) <0$\bar{1}$1> azimuths on As-covered Si(100) surface tilted 4° toward <011>.

Next, we studied the dependence of reconstruction on crystal orientation by RHEED for (a) (100)±1° , (b) 4°±1° off (100) toward <01$\bar{1}$>, (c) 2° off (100) toward <011> and (d) 2° off (100) toward <001> orientations. For the sample (a), the RHEED pattern showed 2x2, which is mixture of 1x2 and 2x1. On the other hand, for the sample (b), the reconstructed structure was 2x1. The RHEED pattern of the sample (c) also showed 2x1 structure, which was not clear as that of the sample (b). In order to get clear single domain 2x1 in the sample (c), the higher annealing temperature may be required, considering from the recent result[10] that the 1000 °C annealing makes a well-oriented (100) surface be a stable 2x1 single domain. The RHEED pattern of the sample (b) indicates that the misorientation should be toward <011> for generation of 2x1 single domain surfaces.

3-2 Initial growth mechanism

For the growth of single domain GaAs, it is important that the Si surface has two atomic height of steps,[11] and that the Si surface is exposed to As flux before GaAs growth is started.[12] The auger signal intensities of Si substrate exposed to As flux indicate that there is one monolayer of As on Si surface. The As layer is stable up to about 700 °C. This result indicates that the first layer on Si probably consists of predominantly Si-As bond. Just after the Ga shutter is opened, the streaky RHEED pattern turns to spotty one and as the GaAs thickness increases, it turns to streak one. This observation indicates that three dimensional GaAs islands grow on Si at first. As the epitaxy goes on and the interfacial energy due to lattice mismatch is released, usual monolayer-growth come about.

In order to know the dimension of the island, the Auger signal intensities of As (=1229eV) and Si (=92eV) were examined at various film thicknesses. The intensities of AES at the substrate temperatures of 80, 350 and 550 °C are shown in Figs. 2(a), (b) and (c), respectively. The AES intensities of Si and As are normalized to that of As-exposed Si surface and that of the clean GaAs surface, respectively. The solid lines in Fig. 2(b) are the expected values calculated

from the growth rate assuming that the epitaxy mode is monolayer growth. The calculation are enable with the equation $I=\exp(-d/\lambda\cos\theta)$, where d, θ and λ are the thickness of the deposited layer, the angle of electron emission to the surface normal (42° determinded by the geometrical configuration of the detector)[13,14], and the escape depth of auger electrons determined as 0.6 nm by several experiments[15]. As shown in Fig. 2(b) the experimental values are quite different from the calculated values. For the growth temperature of 350 °C, Si auger signals were detected until the average of GaAs thickness becomes 50 monolayers, indicating the undulation of 10-15 nm. When the growth temperature increased to 550 °C as shown in Fig. 2(c), the GaAs islands remain up to 60 nm, and the sample has a milky surface. The surface morphology is not improved after deposition of 1 μm epitaxial film. Also, the surface of GaAs at that condition already milky. In Fig. 2(a), auger signal of Si was not detected beyond the thickness corresponding to approximately 15 monolayers of GaAs. The RHEED pattern of GaAs grown at a temperature of 80 °C was spotty until a few monolayer of GaAs was grown and then it changed to hallow pattern indicating that the film was amorphous. After the deposition of 15 monolayer at 80 °C , the sample was heated up to 550 °C under As flux. The amorphous RHEED pattern turned to spotty one with rising the substrate temperature. The AES intensity of As and Si at this temperature are shown in Fig. 2(a). The closed circle is for As, and the closed triangular is for Si. Although the Si intensity is increased a little, the amplitude of the undulation is estimated to be less than 4 nm. Therefore, lowering of the growth temperature at the initial stage is required to obtain the smooth morphology of GaAs layer.

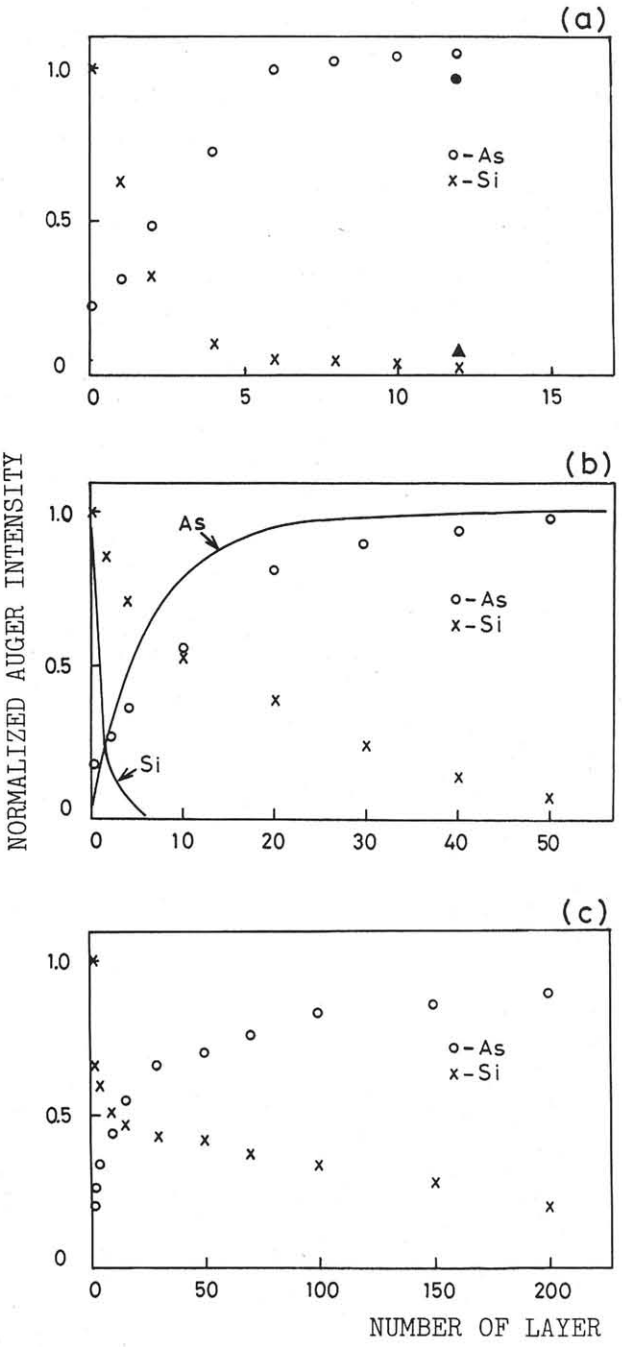

Fig.2. As and Si AES intensities on Si substrate covered with GaAs of different thickness. Growth temperatures are (a) 80°C, (b) 350°C and (c) 550°C. ▲ and ● in (a) are AES intensites of Si and As after the GaAs film are heated up to 550°C. Solid lines in (b) are calculated values of the monolayer growth.

3-3 HRTEM observation of the lattice defect

The imaging of GaAs/Si layer, performed at 400 kV, is shown in Figs. 3 and 4. The growth

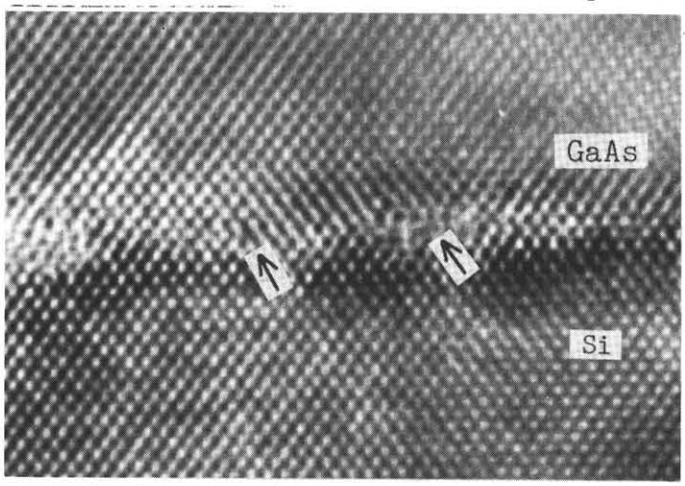

Fig.3. Cross-sectional lattice image in the vicinity of the Si-GaAs interface.

temperature of GaAs was 350 °C. The electron beam was parallel to <011>. The high resolution images were obtained at under focus condition of about 90 nm (Scherger condition), where the images could be interpreted intuitively.

As shown in Fig. 3 the lattice structures do not match perfectly at the interfacial layer. A misfit dislocation (indicated by an arrow) due to 4% mismatch between Si and GaAs is clearly observed. The dislocation existed at every 19 lattices on the average.
These dislocations are probably created for lower the interfacial energy as the GaAs islands on the Si surface expand and meet each other.

Figure 4 shows the undulation of GaAs surface. We put a thin AlAs layer in the GaAs epitaxial layer to confirm that the surface undulation is due to islanding and not due to sputter etching during the sample preparation. The GaAs and AlAs layers were grown at 350 °C. The undulation of GaAs surface and AlAs layer are discribed almost parallel. This image indicates that the undulation of islands can be manifested by an amplitude of about 10 nm. This result agrees approximately with those of AES experiment as shown in Fig. 2(b). Furthermore, several stacking faults and micro-twin boundary, originated from the interfacial layer and grided to (111) plane, can be seen in the GaAs layer. This can be attributed to the difference in lattice constants and to contaminants on the Si surface.

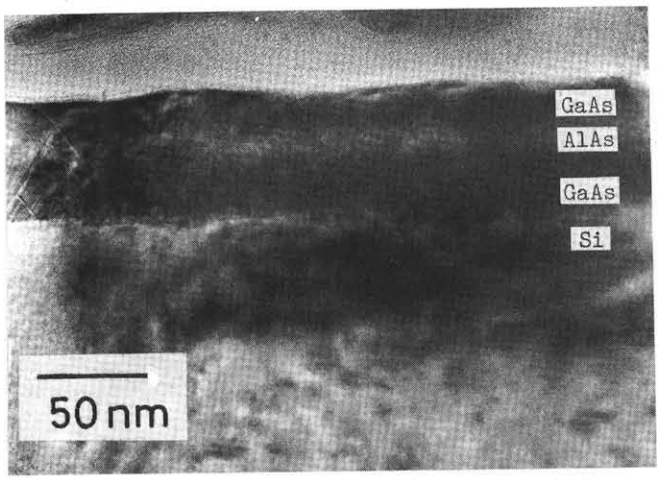

Fig.4. Stacking faults, micro-twin boundary, and surface undulation of GaAs/AlAs layer on Si.

4. Conclusion

For single domain epitaxial film of GaAs on Si, off (100) toward <011> substrate orientation is required. The clean Si surface is covered with one monolayer of As, and the As layer is stable up to about 700 °C. The surface undulation at the initial stage of the epitaxy strongly depends on the growth temperature. Several lattice dislocations can be seen in the vicinity of the interface by HRTEM. These dislocations can be attributed to a difference in lattice constants and to contaminants on the Si surface.

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