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Heteroepitaxy of GaAs on Si Grown by MOCVD and MBE

Masahiro Akiyama

Research Laboratory, Oki Electric Industry Co.,Ltd.

550-5 Higashiasakawa, Hachioji, Tokyo 193, Japan

Single domain GaAs layers are directly grown on Si wafers by MOCVD and MBE with a two-step growth sequence. The grown layers show a fairly high quality such as a mirror-like surface, high electron mobility, low etch pit density and fairly high photoluminescence intensity. The lattice mismatch between GaAs and Si is relaxed in the narrow region near the interface. The domain property of a GaAs layer is determined by the offset angle and the direction of the Si substrate.

1. Introduction

In recent years, the heteroepitaxial growth of GaAs on Si has been studied by many groups and device quality GaAs layers have been obtained by MOCVD and MBE.[1-8] Electrical and optical devices have been fabricated on GaAs/Si wafers,[9-16] and have showed fairly high properties. In these devices, FETs have showed almost the same characteristics as those of the devices on GaAs wafers. In the growth of GaAs on Si, there are two main problems. One is the large lattice mismatch between these materials and the other is the polar on nonpolar problem, i.e., the formation of an antiphase domain structure To solve the problem of the lattice mismatch, Ge buffer layer has been used. To solve the polar on nonpolar problem, the use of (211)-oriented Si substrates was proposed.[5] Recently, it was reported that the composite strained layer superlattice with GaP/GaAsP and GaAsP/GaAs was effective to solve the both problems.[8] Another method to solve the problems is the direct growth of GaAs on Si. In the direct growth, we reported that a two-step growth sequence was very effective.[6-7] This growth technique is a very simple method to grow a high quality GaAs layer on a Si substrate. However, the grown layers still have problems such as a wafer bending because of the tensile stress due to the difference in the thermal expansion between GaAs and Si, and the short diffusion length of the minority carriers.[17]

In this paper, the growth sequence of GaAs on Si, the properties of the grown layers are briefly reported. Then, the growth mechanism and some of the still remained problems are discussed.

2. Two-Step Growth

We used MOCVD and MBE for the growth. Epitaxial layers with the same quality were obtained on (100)-oriented Si substrates by both growth techniques with nearly the same growth sequence. The precise sequence was already reported.[6,7] At first, a Si substrate was heated to about 900 ℃. Then, the substrate was cooled to about 450 ℃ or below and a thin GaAs layer of less than 200 Å was deposited. Next, the wafer was reheated to the conventional growth temperature and the second GaAs layer was grown. The two-step growth sequence of this kind had been reported to be useful for other heteroepitaxial growths such as SiC on Si[18] and Si on sapphire.[19]

3. Properties of the Grown Layers

The GaAs layers grown with this two-step growth sequence showed a mirror-like surface. The etch pit pattern by molten KOH is shown in Fig.1. As seen in the figure, all pits have the same direction, indicating that the layer has a single domain structure. Furthermore, a very low etch pit density (EPD) of 1000 - 3000 cm^{-2} was observed. An electron mobility was 5200 $cm^2V^{-1}s^{-1}$ at room temperature with a carrire density of

$1 \times 10^{16}cm^{-3}$. This mobility is comparable to that of a homoepitaxially grown layer. The GaAs and AlGaAs layers showed fairly high photoluminescence (PL) intensities. Figure 2 showes the PL spectra of Zn-doped $Al_{0.32}Ga_{0.68}As$ layers on a Si and on a GaAs substrate. These layers were grown simultaneously on a 3000 Å thick GaAs coated Si and on a GaAs substrate. The intensities are nearly the same. In the C - V measurement, a thin GaAs layer showed an n-type conductivity with an electron density of more than $10^{18}cm^{-3}$ near the GaAs/Si interface. And the electron density decreased steeply from the interface to the surface.

4. Growth Mechanism

There are two points we have to make clear. One is how the lattice mismatch is relaxed and the other is how a single domain GaAs layer grows on a (100)-oriented Si substrate. In a RHEED study, the thin GaAs layer deposited at low temperatures showed an amorphous pattern or a pattern containing many twins. The pattern, however, changed to the complete single crystalline one after the annealing at the conventional growth temperature. In a MBE growth, it was also confirmed that the direction of the grown layer had been determined after the annealing.

Figure 3 shows the TEM photograph of the lattice image near the GaAs/Si interface. In this figure, we can see the lattice turbulence occurs in a few atomic layers at the interface. Along the interface, two kinds of small regions are observed. One is the region where the lattice turbulence is small (indicated by arrow A), and the other is the region where the strong turbulence is seen (arrow B). These two kinds of regions are arranged periodically and we can observe about 25 lattice points in one span of the periodicity. In Fig. 4, the periodicity is seen more clearly. Furthermore, a moire pattern is observed in plane view as shown in Fig. 5.[20] From these TEM observations, the lattice mismatch is thought to be relaxed in the narrow region at the interface when the GaAs layer is grown by the two-step growth sequence. The mechanism is thought as follows. The first GaAs layer deposits with its own lattice constant. At this stage, there may be two kinds of regions, i.e., the regions relatively

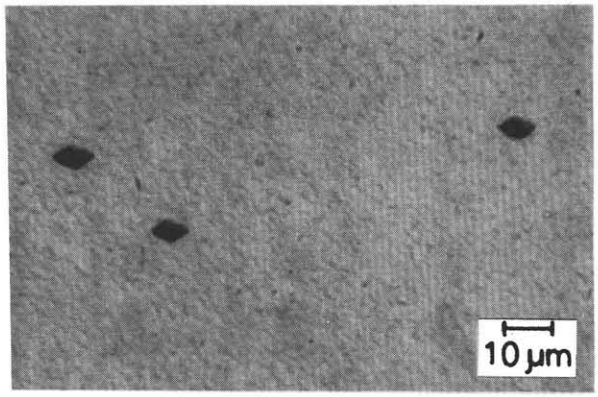

Fig.1. Etch pit pattern of a GaAs layer on a Si substrate.

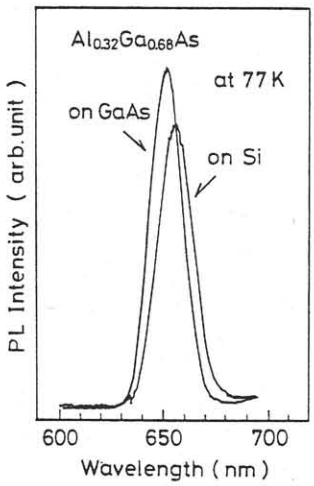

Fig.2. PL spectra of Zn-doped $Al_{0.32}Ga_{0.68}As$ layers on a GaAs and on a Si substrate.

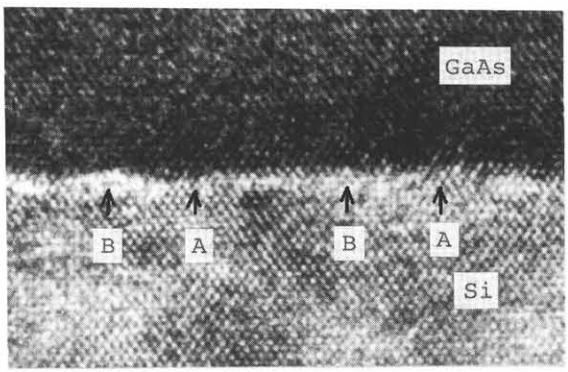

Fig.3. Lattice image near the GaAs/Si interface.

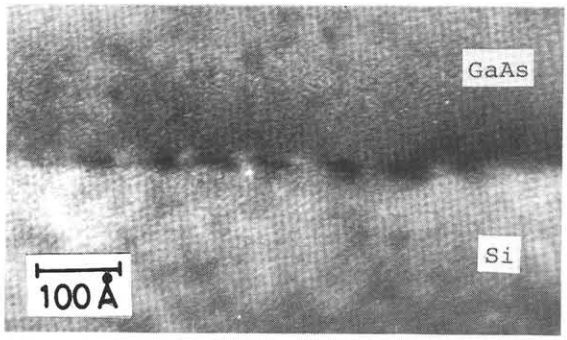

Fig.4. Cross-sectional TEM photograph of the GaAs/Si interface.

lattice matched and mismatched to Si. During the annealing, a solid phase epitaxial (SPE) process may occur. In this SPE process, the relatively lattice matched regions may act as seeds. The SPE occurs to lateral directions as well as upwards and the stress due to the lattice mismatch may be confined in the other regions as illustrated in Fig. 6. With this mechanism, the lattice mismatch may be relaxed.

It was reported that Si substrates with an offset angle from (100) are adequate to grow single domain GaAs layers with a good morphology.[4] To make clear the effects of an offset angle of the substrate, the growth on Si substrates with a spherical surface around (100) was performed. Figure 7 shows a photograph of a grown layer and an illustration of the top view. In the illustration, the orientations of the grown layer are indicated which are determined from the shape of the etch pits by molten KOH. The grown layer is divided into four parts and each part has a single domain structure and the narrow regions along the boundary show an antiphase domain structure. The boundary has [001] and [010] direction for the substrate. The cross point of the boundary lines has just a (100) orientation. From this experiment, it becomes clear that the domain property and the orientation of the grown layer are determined by the offset direction of the Si substrate, and a very small offset angle of less than 0.2° is enough to obtain a single domain layer. Commercially obtained (100)-oriented Si wafers have an offset angle of this degree. In a LEED and a RHEED study,[21-23] it was reported that the steps of a vicinal (100) Si surface tilted towards [011] had a biatomic layer height by the surface reconstruction after heat treatment at high temperatures. It was pointed out that the steps with a biatomic layer height were suited to grow a single domain GaAs layer.[24] Therefore, the heat treatment of Si substrates prior to the growth is thought to be necessary not only for surface cleaning, but also for obtaining a reconstructed surface. Our experimental results suggest that a Si reconstructed surface has only biatomic layer steps and all bonds of the surface have a same direction in the whole region where a single domain GaAs layer is grown.

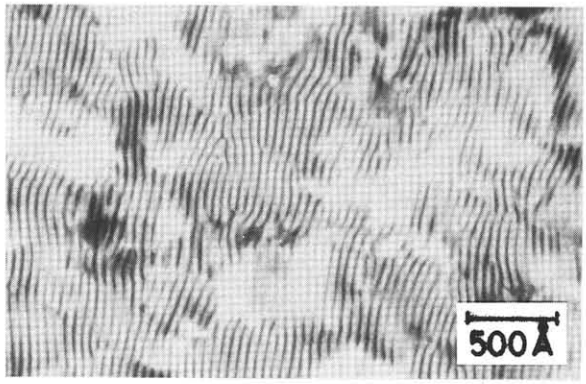

Fig.5. TEM photograph in Plane view of GaAs/Si.

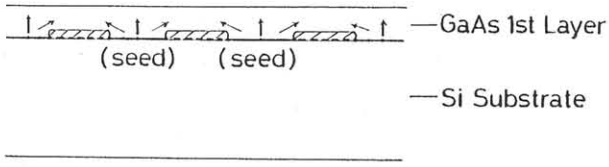

Fig.6. SPE process of the first GaAs layer during annealing.

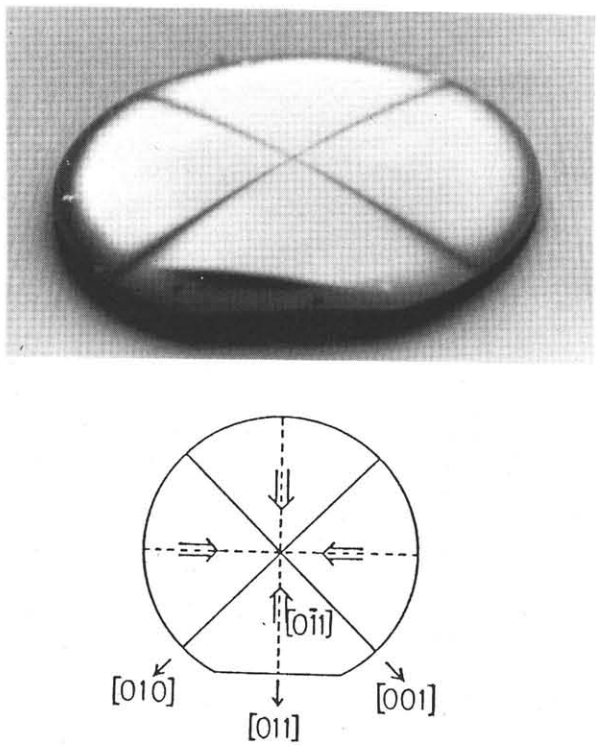

Fig.7. Photograph of a GaAs layer on a Si substrate with a spherical surface and an illustration of the top view.

5. Problems

Fairly high quality GaAs layers are grown on Si substrates. However, some problems still remain in this system. The efficiency of the light emitting diodes is still lower than that of the devices on GaAs substrates. A laser diode of CW operation at room temperature has not been reported yet. As shown in Fig.1, a surface roughness is observed after etching by molten KOH. Such a rough surface is not seen on GaAs wafers. The origin is not clear now. However, it may related to some defects. It was reported that the diffusion length of the minority carriers was shorter than that in homoepitaxially grown GaAs layers.[17] These unknown defects may affect the diffusion length of the minority carriers.

The thermal expansion coefficient of GaAs is about two times larger than that of Si. Therefore, a tensile stress comes arise to the GaAs layer when the wafer is cooled after the growth. The stress limits the thickness of the grown layer and bends the wafer. To reduce the wafer bending, a selective or an embeded growth will be effective. We tried these growths by reduced pressure MOCVD and found that the growths occured on Si wafers with the same manner as on GaAs wafers. The GaAs did not show any cracks with the thickness of up to 8 μm with each grown area of 300 x 300 μm^2 (750 μm pitch). The wafer bending was much reduced to about 20 % of that of the uniformly grown wafer with the same layer thickness.

6. Summary

Single domain GaAs layers are directly grown on Si substrates. The lattice mismatch between GaAs and Si is relaxed in the narrow region near the interface. The domain property of a GaAs layer is determined by the offset angle and the direction of the Si substrate. The grown layers show a fairly high quality such as a mirror-like surface, high electron mobility, low EPD and fairly high photoluminescence intensity. The GaAs/Si system has possibilities to fabricate new types of devices. However, some problems still remain in the system. It is necessary to solve these problems for GaAs/Si wafers to be used widely.

7. Acknowledgement

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8. References

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