GaAs Inversion-Base Bipolar Transistor (GaAs IBT): Future Transistor of Completely New Principle

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A GaAs bipolar transistor with a SIS FET-like structure and with its base formed by two-dimensional hole gas was first fabricated. Since the transistor has an extremely thin inversion hole layer working as a base layer, the transistor is expected to exhibit extremely good high-frequency/ high-speed characteristics. The current gain of β =5.6 at 77K and β =17.1 at 300K was obtained in the common-emitter mode.

§1. Introduction

The high electron-mobility property and the band-engineering capability of III-V compound semiconductors have atracted device people to try and apply the materials for various highhigh-speed devices. hetero-junction bipolar transistors (HBT) and hetero-junction FETs (e.g. HEMTs) the examples of such devices.

Hetero-junction FETs are already in practical use as high frequency amplifiers and are also under development as LSIs (e.g. 4Kb-SRAM). Also, a hetero-junction FET of a Si MOSFET analogy, SIS FET, has been reported by the present authors 1).

On the other hand, HBT are still in the developmental stage. Main reasons for a rather peculiar to compound semiconductors. and highly doped $(\simeq 10^{19}/\text{cm}^3)$ semiconductor. sandwiched between other kinds of semiconductor. has been the source of many limitations.

Another important aspect of HBTs which we would like to see developed, and which is lacking with the present HBT technology, is the compatibility of the fabrication technology with that of hetero-junction FETs. If this could be realized, we would have FET/bipolar integrated circuits as we already have MOSFET/bipolar integrated circuits with the Si technology.

In the present paper, we propose a completely new type of GaAs bipolar transistor with a base formed by two-dimensional inversion hole gas. this new transistor Inversion-Base Bipolar Transistor (GaAs IBT)". The base thickness of the GaAs IBT corresponds to that of the inversion layer which is more than ten times thinner than that of a conventional GaAs HBT. The base resistance remains low owing to the high hole-density and to the high hole-mobility²⁾ in the inversion layer. Furthermore, the fabrication process is easier compared to that of the GaAs HBT, and is almost the same as that of a GaAs SIS FET. Therefore, the GaAs IBT is very likely to be employed in future GaAs-based high-speed integrated circuits.

slow progress lie in the technical difficulties in crystal growth and fabrication process Especially, a base layer of a very thin (≥1000Å)

Nevertheless, we would like to see the thickness of the base layer further reduced without reducing the sheet conductivity of the layer for better high-frequency/high-speed performances.

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§2. Device structure

The structure of the GaAs IBT is shown in Fig.1. The transistor has an n⁺-GaAs layer as an emitter, an n⁻-GaAs layer as a collector, an undoped thin AlAs layer between them, and has a self-aligned external-base p⁺-GaAs region. The most significant feature of the GaAs IBT is that there is no metallurgical base-layer present, and that an undoped thin AlAs layer is present between the emitter and the collector layers.

§3. Principle of operation

Fig.2 shows the energy-band diagram of the GaAs IBT in which the emitter-base bias of V_{EB} =1.8V and the base-collector bias of V_{BC} =0V are applied in the common-base mode. The emitter-base bias of more than V_{EB} =1.8V is necessary for the GaAs IBT of a particular dimension discribed in §4 to exhibit the transistor action. The bias of V_{EB} =1.8V, which consists of the bias across the AlAs layer of 0.4V and the surface potential of the n-GaAs collector of V_{S} =1.4V, makes the surface of the n-GaAs collector at the n-GaAs/AlAs interface inverted. The strong inversion hole layer thus formed is connected with the external-base p⁺-GaAs layer.

In fact, at the emitter-base bias of more than $\rm V_{EB}$ =1.8V, the current was observed to flow between the two biased external-base regions

Emitter

WN

Base

n+-GaAs

p+-GaAs

Inversion Layer

n--GaAs

HB: n+-GaAs Sub.

Collector

Fig.1 Schematic structure of GaAs Inversion-Base Bipolar Transistor (GaAs IBT)

(the external-base region is divided into two regions as shown in Fig. 1), and the device showed FET characteristics.

The inversion hole layer thus formed works as an extremely thin base layer of the GaAs IBT. The valence band discontinuity at the n-GaAs/AlAs interface is so high $(\Delta E_V = 0.5 \text{eV})^3$ that the holes are confined at the interface. The electrons in the n⁺-GaAs emitter, which have a lighter mass, can tunnel through the thin and low $(\Delta E_C = 0.2 \text{eV})^3$ AlAs barrier-layer, pass through the inversion base layer and reach the collector after falling down the slope of the collector depletion layer.

Any increase of the emitter-base voltage beyond $V_{\rm EB}$ =1.8V is applied not to the collector depletion layer but to the AlAs barrier layer, because the collector layer is shielded by the inversion hole layer. Therefore, the increase in the emitter-base bias is used only to make thinner the triangular potential-barrier of the conduction band, which increases the electrons that can tunnel through the AlAs barrier layer and increases the collector current.

By changing the base-collector bias V_{BC} , the collector current is not modulated. This is because the change of the base-collector bias V_{BC} is used only to modulate the collector depletion layer and is not used to modulate the triangular potential-barrier of the conduction band. This is again due to the shielding effect of the inversion hole layer at the AlAs/n-GaAs interface.

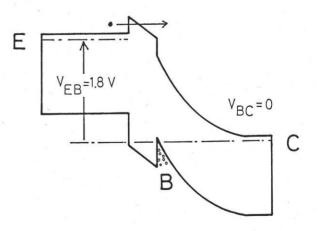


Fig.2 Energy-band diagram of GaAs IBT in commonbase mode at $\rm V_{EB}\mbox{=}1.8V$ and $\rm V_{BC}\mbox{=}0V$

§4. Device fabrication

The crystal used was grown by MBE, and has the following structure: HB n+-GaAs substrate (Si doped, $300\mu\text{m}$)/n-GaAs (Si doped, 1×10^{16} /cm³, 1.5µm)/undoped AlAs (100Å)/n+-GaAs (Si doped, $1\times10^{18}/\text{cm}^3$, 5000Å). A 5000Å tungsten-nitride (WN) layer was deposited by sputtering technique on the top n+-GaAs. The WN layer and the n+-GaAs layer were selectively etched to form an emitter of 50µmx50µm. Using the WN and the n⁺-GaAs layers as a mask, magnesium (Mg) ions were implanted to form the self-aligned external-base p -GaAs region. The sample was then flash annealed at 800 °C for 30 seconds without a cap under an arsenic pressure. Ohmic electrodes were formed to the top n+-GaAs, the ion implanted p+-layer and the back side of the HB GaAs substrate for the emitter, base and collector electrodes, respectively.

§5. Experimental results

Fig.4 shows the transistor characteristics measured at 77K in the common-base mode. The collector current $\rm I_C$ increases almost uniformly with a constant emitter current step, and reaches $\rm I_C=7.5mA$ or $\rm I_C=3x10^5mA/cm^2$ at $\rm I_E=10mA$. The current gain is $\rm C I_C=0.8$. The collector current $\rm I_C$ begins to decrease rapidly at around the base-collector bias of $\rm V_{BC}=-1.2V$. This is due to the current flowing through the forward-biased base-collector pn-junction.

Fig.5 shows the transistor characteristics in the common-emitter mode at 77K. The collector

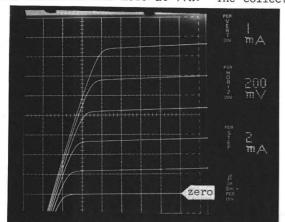


Fig.4 Collector current vs. base-collector bias characteristics of GaAs IBT in common-base mode at 77K.

Emitter current increases from OmA to 10mA with 2mA step.

current reaches $I_C=9mA$ or $I_C=3.6x10^5mA/cm^2$ at the base current of $I_B=2mA$. The current gain is $\pmb{\beta}=5.6$.

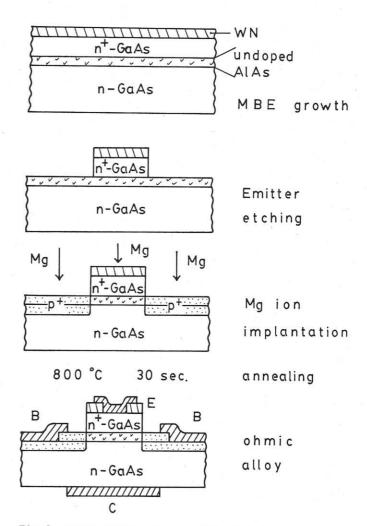


Fig. 3 Fabrication steps of GaAs IBT

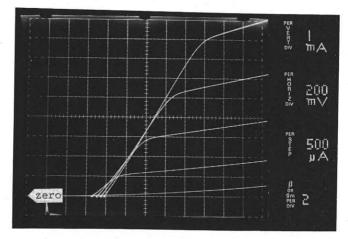


Fig.5 Collector current vs. emitter-collector bias characteristics of GaAs IBT in common-emitter mode at 77K.

Base current increases from OmA to 2mA with 0.5mA step.

The transistor also worked at 300K, and showed the current gain of d = 0.92, and B=17.1 in the common-base and common-emitter modes as shown in Figs.6 and 7, respectively. common-emitter mode, the collector In the current reaches $I_{C}=39\text{mA}$ at $I_{B}=2\text{mA}$, corresponds to $I_c=1.56 \times 10^6 \, \mathrm{mA/cm}^2$, and is about five times larger than that at 77K. increase of the current gains d, β , and of the collector current I at 300K than at 77K is due to the increase of the number of the thermally-stimulated electrons which can go over the AlAs barrier from the n -GaAs emitter to the n -GaAs collector.

§6. Conclusion

We have fabricated the first GaAs bipolar transistor with the base formed by an inversion hole layer. The transistor worked exactly in a manner expected from the principle of operation. The current gains were $\alpha=0.8$ and $\beta=5.6$ at 77K, and $\alpha=0.92$ and $\beta=17.1$ at 300K for the common-base and common-emitter modes, respectively.

The Authors wish to thank Dr. T. Tsurushima for his continuous encouragement for the present work. They are also indebted to Prof. K. Tomizawa, Prof. T. Kurosu, and Prof. M. Iida for their helpful suggestions.

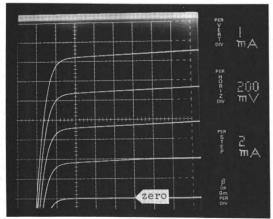


Fig.6 Collector current vs. base-collector bias characteristics of GaAs IBT in common-base mode at 300K.

Emitter current increases from OmA to 10mA with 2mA step.

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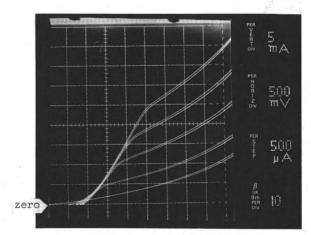


Fig.7 Collector current vs. emitter-collector bias characteristics of GaAs IBT in common-emitter mode at 300K.

Base current increases from OmA to 2mA with 0.5mA step.