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Self-Aligned AlGaAs/GaAs HBTs and 35 ps LCML Ring Oscillators Fabricated by Mg and P Double Implantation

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The influence of the lateral diffusion of implanted Mg on HBT characteristics was examined. It was found that Mg and P double implantation suppresses the lateral diffusion of Mg. This method is effective to realize a small size emitter in HBTs. Self-aligned emitter/base contact fabrication was carried out. These transistors were used to construct LCML ring oscillators with 35ps gate delay time.

1 Introduction

Heterojunction bipolar transistors have been widely expected to have a great potential for use in ultra-high speed logic devices[1]. In principle, there is no doubt regarding this expectation, but actual device performances realized up to now[2,3] have been considerably inferior to the expected performances in ideal HBTs. This large discrepancy, existing between actual and ideal status, is mainly due to the large device size and large values of parasitic elements. Therefore, many recent papers have paid specific attention to the self-alignment technology for achieving fine pattern structures and the reduction of parasitic elements[4,5,6].

Regarding device size reduction, two problems will be described in this paper. One is the lateral diffusion of acceptors, which are implanted into the external base region. The other is a self-alignment technique for both emitter and base electrode formations. After the examination of these problems, transistor characteristics and ring oscillator performance will also be demonstrated.

2 External base fabrication

Although acceptor implantation is a widely used process in fabricating HBTs to form a thick, low resistivity external base region, it is well known that group two element acceptors diffuse very rapidly in GaAs and AlGaAs. This section presents the influence of lateral diffusion of implanted acceptors on transistor characteristics and an ion implantation technique to minimize acceptor redistribution.

To examine the degradation in transistor characteristics caused by size reduction, HBTs with different emitter areas were fabricated. The MBE grown wafer structure used for the tested devices is shown in Table 1. Conventional non self-aligned processes were adopted. Mg was implanted into the external base region at 150 keV with 2.6×10^{14} cm^{-2} dose. Post-implant annealing was carried out in an infrared lamp furnace at 890℃ peak temperature. Emitter areas were varied from 20 μm square to 5 μm square. The offset voltage in the emitter grounded configuration and the current gain were measured as a function of emitter size. Measured results are shown in Fig.1. The horizontal axis is the ratio of emitter periphery length to emitter area. As the emitter size decreased, the offset voltage increased markedly, whereas the current gain decreased. This degradation in transistor characteristics with size reduction is assumed to be caused by the lateral diffusion of implanted acceptors at the emitter periphery.

In the grown wafer structure, there was a 30 nm thick n-type composition grading layer at the emitter-base interface. Thus, the conduction band

spike in the AlGaAs-GaAs heterojunction system was eliminated. However, when the implanted acceptors diffuse laterally into the intrinsic emitter region, the p-n junction moves into the wide gap emitter region. This misplacement between the p-n junction and the heterojunction causes a conduction band spike at the emitter base junction. As a result, the turn-on voltage increases and the injection efficiency decreases at the emitter periphery. In large emitter devices, lateral diffusion of the acceptors can be neglected. For example, in a 20 μm square emitter transistor, the turn-on voltage was less than 0.1 V and the current gain was higher than 100, as shown in Fig.1. On the other hand, in a small size device, i.e. 5μm square emitter, the turn-on voltage increased up to greater than 0.3 V, which is almost equal to the bandgap difference between $Al_{0.3}Ga_{0.7}As$ and GaAs. As a result, the benefit of a wide gap emitter was missed and the current gain decreased to 12.

To overcome this problem, double implantation of Mg and P was examined. Figure 2 shows the carrier profiles for Mg-only implanted and Mg and P double implanted GaAs layers. Mg was implanted at 150 keV with $2.6\times10^{14}cm^{-2}$ dose, and P was implanted at 190 keV with the same dose. Anomalous diffusion of Mg was observed in Mg-only implanted GaAs, while it was significantly reduced in double implanted GaAs layers. From these experiments, anomalous rapid diffusion of Mg is interpreted as a behavior similar to the interstitial-substitutional diffusion of Zn in GaAs[7]. The added P produces Ga vacancy and enhance the substitution of Mg for the Ga site. As a result, rapid diffusion of interstitial Mg is suppressed in the double implanted layers. Although a similar effect of suppressing anomalous diffusion was observed in the cases of Zn and As or Zn and P double implantation into a GaAsP mixed crystal[8], the Mg and P combination is more suitable for fabricating a deep external base region in HBTs.

Mg and P double implantation was applied to form the external base regions for the HBTs. Figure 3 shows the offset voltage and the current gain in an emitter grounded configuration as a function of emitter size. Compared with Mg-only implanted HBTs, the increase in offset voltage was significantly suppressed. Rapid decrease in current gain through the reduction of injection efficiency, as observed in Fig.2, was also suppressed. Surface recombination current at the emitter periphery may be responsible for the gradual decrease in current gain in Fig.3. From these experimental results, it has been confirmed that the double ion implantation technique is very effective to suppress the lateral diffusion of implanted acceptors and that it will be one of the key technologies to realize still smaller size HBTs.

3 Self-aligned contact formation

Figure 4 shows a cross-sectional view of a completed self-aligned HBT. In this structure, submicron spacing between the emitter and base electrodes was attained. Because of the overlaid structure of the emitter electrode, the emitter width can be reduced, independently from the alignment margin, for contact formation.

The main fabrication procedure for self-aligned HBTs is described below. The starting material was grown by MBE. The wafer structure was similar to that for conventional ones, except for a considerably thick n^+GaAs top layer for the overlaid contact structure. The n^+GaAs top layer was 400 nm thick. By using CVD-SiO_2 as a mask, the n^+GaAs top layer was etched by reactive ion etching in CCl_2F_2 plasma. The etching was stopped at the AlGaAs surface, due to the high etching selectivity between AlGaAs and GaAs in CCl_2F_2 gas[9]. Subsequently, Mg and P were implanted into the external base region and annealed in an infrared lamp furnace with a SiO_2 capping layer (Fig.5(a)). After annealing, boron ions and protons were implanted to form isolation regions. In the next step, the SiO_2 layer was etched away from the wafer surface by reactive ion etching, while the first thick SiO_2 mask and the side-wall of the emitter mesa were still left (Fig.5(b)). Then, the base metal of AuZn was evaporated and lifted off by dissolving SiO_2, which covered the emitter mesa. The spacing between the base metal and emitter region was determined by the SiO_2 side-wall thickness, i.e. 0.25 μm in this work. After field SiO_2 deposition, the wafer surface was flattened by coating photoresist, as shown in Fig.5(c). The photoresist and SiO_2 were etched at an equal rate in CF_4 and O_2 mixed gas plasma until the n^+GaAs

emitter mesa was exposed. Finally, a AuGeNi ohmic metal was deposited on the emitter mesa (Fig.5(d)).

4 Transistor characteristics

Figure 6 shows current-voltage characteristics for a self-alignment HBT with 2.6 × 3.6 μm emitter area. A current gain of about 30 was observed. No degradation was found in transistor characteristics, due to the self-alignment technology, compared with the conventional processes. For the same emitter area devices, the current gains in self-aligned HBTs were almost equal to those in transistors fabricated by conventional processes.

To test the switching performance of these self-aligned HBTs, 31-stage low level current mode logic (LCML) ring oscillators were fabricated. The circuits were tested under the following conditions; logic swing was from 0.4 V to 0.6 V and supply voltage was -4 V. Figure 7 shows a micrograph of a completed circuit and a representative oscillation waveform. In ring oscillator RO1, which was constructed by 1.6×3.6 μm emitter transistors, a 37ps gate delay time was obtained at 5.9 mW/gate. In RO2, constructed by 2.6×3.6 μm emitter transistors, a 35ps minimum gate delay was obtained at 11.4 mW/gate. SPICE circuit simulation was carried out, based on the parameters in Table 2. Simulated delay times were 38ps and 37ps per gate for RO1 and RO2, respectively. These results agreed well with the experimental results. From the simulation, it was found that switching speed strongly depended on base-collector capacitance in these devices. Though a 2 μm alignment margin for defining the base-collector junction area was adopted in this work, a less than 20ps gate delay time was expected for 1 μm rule self-aligned HBTs.

5 Conclusion

The influence of the lateral diffusion of implanted Mg on HBT characteristics was examined. It was found that Mg and P double implantation suppress the lateral diffusion of Mg. This method was confirmed to be a key technology for use in realizing small size HBTs. Self-aligned emitter/base contact formation was developed. By using this technique, 1.6 μm emitter width and a quarter micron spacing between the emitter and base were achieved. LCML ring oscillators, implemented with these self-aligned HBTs, were also fabricated. A very high switching speed, 35 psec, was obtained.

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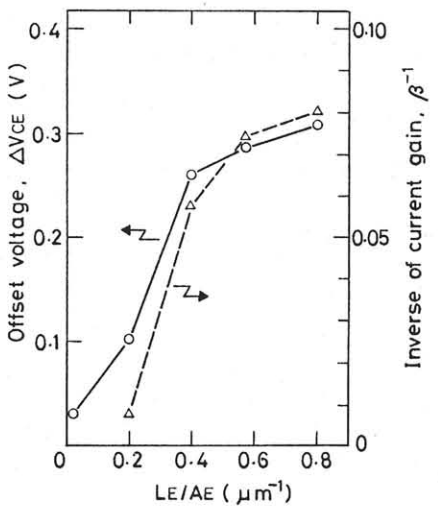

Fig.1:Collector-emitter offset voltage and inverse of current gain vs. emitter size. External base was formed by Mg-only implantation. Current gain was measured at 10kA/cm² collector current density.

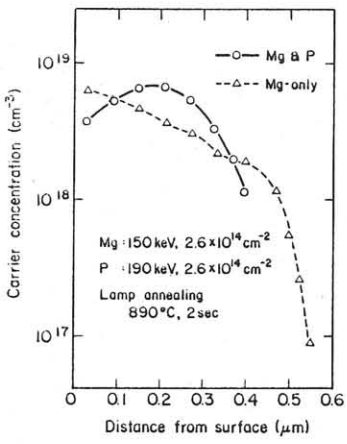

Fig.2:Depth profiles of carrier concentration for Mg-P and Mg-only implanted GaAs layers.

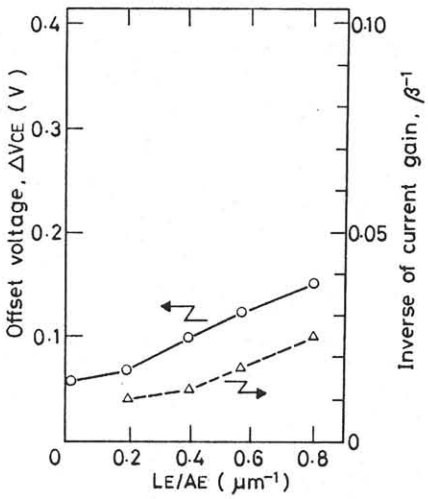

Fig.3:Collector-emitter offset voltage and inverse of current gain vs. emitter size. External base was formed by Mg and P double implantation. Current gain was measured at 10kA/cm² collector current density.

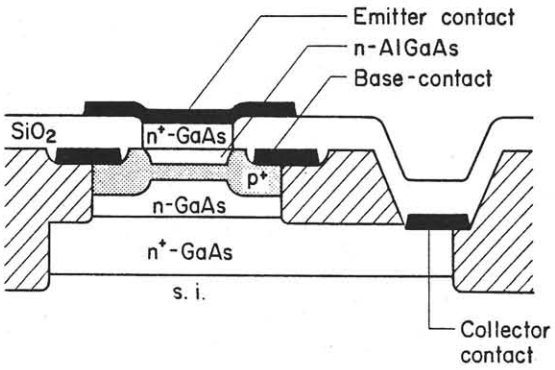

Fig.4:Self-aligned HBT cross-sectional view.

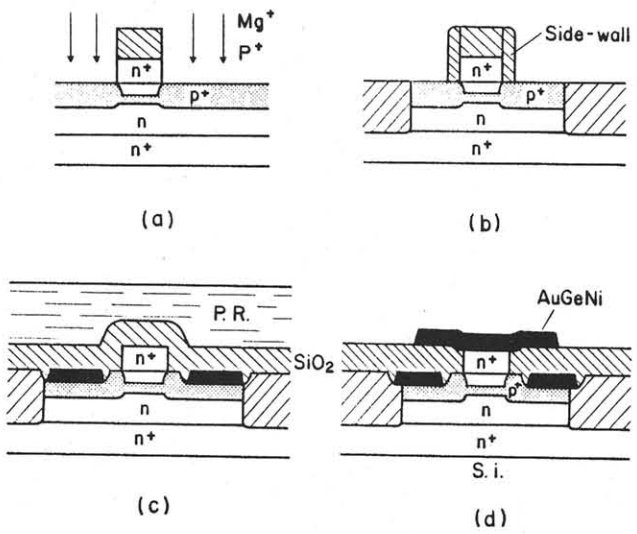

Fig.5:Fabrication procedure for self-aligned HBTs.
(a)External base implantation.
(b)Side-wall formation.
(c)Surface flattening.
(d)Emitter ohmic metallization.

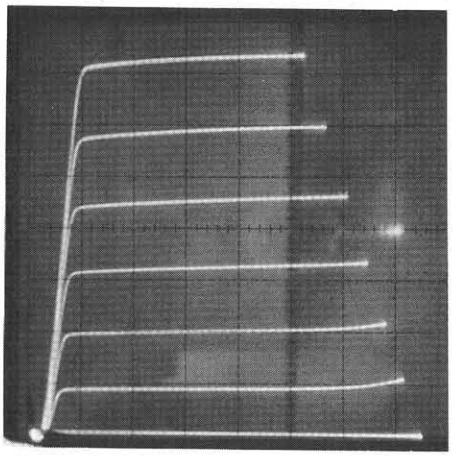

Fig.6:Emitter grounded I-V characteristics.
Ic:0.5mA/div., Vc:1V/div., Ib:20μA/div.

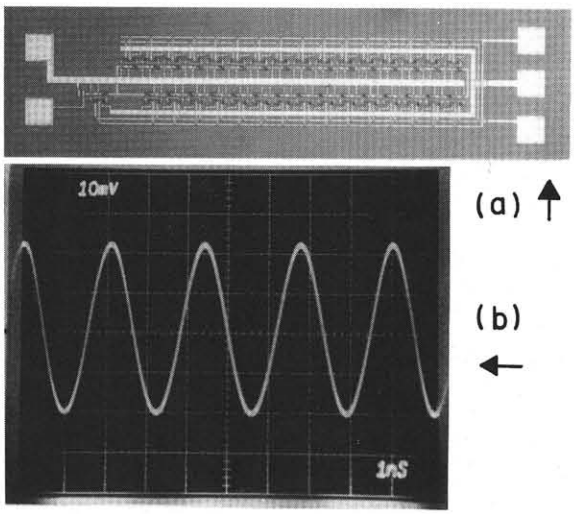

Fig.7:(a)31-stage ring oscillator micrograph.
(b)Oscillation waveform corresponding to 35ps gate delay time.

Layer		Doping (cm^{-3})	Thickness (nm)
Cap	n-GaAs	5.0E18	100
Grading	n-AlGaAs	5.0E18	30
Emitter	n-$Al_{0.3}Ga_{0.7}As$	2.5E17	190
Grading	n-AlGaAs	2.5E17	30
Base	p-GaAs	1.0E19	120
Collector	n-GaAs	5.0E16	400
Sub collector	n-GaAs	2.0E18	480

Table 1:MBE wafer structure.

		RO1	RO2
A_{EB}	(μm^2)	1.6 x 3.6	2.6 x 3.6
A_{CB}	(μm^2)	6 x 8	7 x 8
R_E	(Ω)	76	42
R_B	(Ω)	32	43
R_C	(Ω)	42	42
C_{EBJ}	(fF)	9.4	15.4
C_{CBJ}	(fF)	25.1	30.3
τ_F	(ps)	3.0	3.0
R_L	(Ω)	300	200
t_{pd}	(ps)	38	37

Table 2:SPICE modeling parameter.