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Novel Heterostructure Transistors with Extremely Small Separation between Gate and Channel

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We describe heterostructure FETs with the metal-to-channel spacing of only 100Å to 400Å: inverted FETs with transconductance of 1810 mS/mm at 77 K and 1180 mS/mm at 300 K, Superlattice Modulation Doped FETs and Complementary Heterostructure Insulated Gate FETs . Digital HIGFET and SL-MODFET ICs have gate propagation delays as short as 22 pS . Small variation of threshold voltage across the wafer and with temperature and the insensitivity of the device characteristics to light were observed.

In this paper we describe a new generation of high performance heterostructure transistors with the metal-heterojunction interface spacing of only 100Å to 400Å. In particular, we consider three new types of devices - Complementary Heterostructure Insulated Gate Field Effect Transistors (CHIGFETs) [1], Superlattice Modulation Doped Field Effect Transistors (SL-MODFETs) [2] and Inverted Modulation Doped Field Effect Transistors (IMODFETs) [3].

All these devices are fabricated on MBE grown structures using a self-aligned process. In Fig.1 we show a schematic structure of two complemetary Heterostructure Insulated Gate Devices with n and p-type channels.

Both types of transistors are fabricated using the same MBE grown layer of undoped gallium arsenide on a semi-insulating gallium arsenide substrate followed by the undoped aluminum gallium arsenide layer. An ion implantation process is used to fabrication the n^+-doped contact regions for n-channel devices and p^+-doped regions for p-channel devices. No dopants are used in the active region itself. Hence, these devices are, in effect, just dielectric films with contacts. The band discontinuities at the heterointerface provide potential wells where two-dimensional electron and hole gases are induced in n and p channel devices respectively. The devices are fabricated on the same

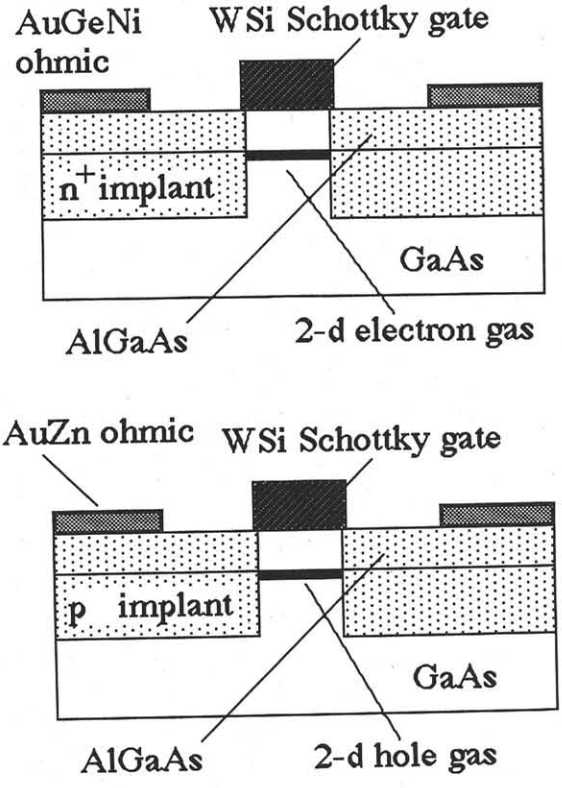

Fig.1 Schematic HIGFET structure

planar wafer surface allowing for Large Scale or Very Large Scale Integrated Circuits to be built using this new technology. Short propagation delays have been recently achieved in HIGFET logic

circuits[4]. At the same time the combination of n and p channel devices allows us to achieve very low stand-by power using complementary logic gates.

Recently we presented experimental evidence for negative differential resistance in n-channel HIGFETs at high gate voltages [5]. This negative resistance may be explained by a mechanism similar to that causing the negative differential resistance in so-called Negative resistance Field Effect Transistors (NERFETs) [6,7]. In 1979 Hess et al predicted and then observed so-called "real space transfer effect [8,9]. In a real space-transfer diode electrons are moving in a GaAs layer sandwiched between AlGaAs layers. In high electric fields the electron temperature increases and they are transferred by the thermoionic emission into AlGaAs regions where the electron velocity is low. This mechanism may lead to a negative differential resistance.

In 1983 Kastalski and Luryi proposed a three terminal device (NERFET) based on a similar concept [6]. Again, the increase in the electron temperature with the increase in the drain-to-source voltage leads to the increase in the substrate current and, as a consequence to the drop in the drain-to-source current, i.e. to the negative differential resistance.

The basic advantage of this device is a possibility to achieve a higher speed of operation because the modulation of the drain-to-source current in this regime is related to the electron heating. The change in the electron temperature is limited by the longest of the two time constants: the energy relaxation time (of the order of 1pS or so for GaAs) and the time constant of the electric field variation. The latter time is determined by the electron transit time across the high field region near the drain and may be several times shorter than the transit time of electrons across the gate which sets up a limit for the intrinsic speed of conventional field effect transistors.

Our observation of the negative differential resistance in HIGFETs opens up an opportunity to develop ultra-fast Hot Electron Transistor with very low parasitics.

The second type of novel devices we have developed are Inverted Modulation Doped Field Effect Transistors - IMODFETs. In conventional MODFETs the conducting channel is separated from the gate by an aluminum gallium arsenide layer. In inverted MODFETs the layers are reversed with a gallium arsenide layer being close to the gate. Such devices may have a higher transconductance than conventional "normal" MODFETs[10].

We fabricated high performance inverted MODFETs with the metal-heterojunction interface spacing of only 100Å having a transconductance of 1810 mS/mm at 77 K and about 1180 mS/mm at 300 K [3]. To our knowledge these values are the the highest reported up to date. Moreover, we estimate that they are primarily determined by the series source resistance with actual intrinsic transconductances being higher still.

The third type of novel heterostructure devices - Superlattice Modulation Doped Field Effect Transistors - incorporates narrow doped GaAs quantum wells imbedded into AlGaAs separating the heterointerface from the gate metal. The schematic device structure is shown in Fig.2.

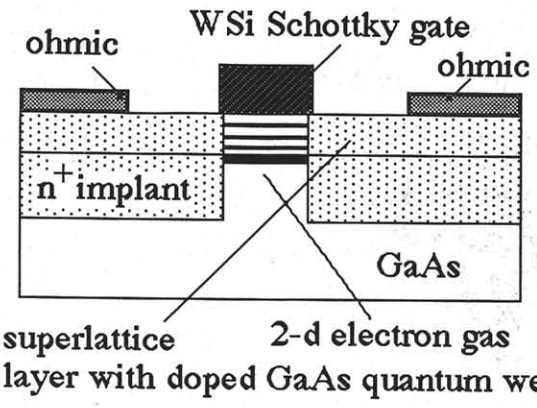

Fig.2 Schematic structure of SL-MODFET.

In these devices the current and voltage swings are enhanced by the parallel conduction in highly doped quantum wells as indicated by pronounced peaks in the the measured dependence of the device transconductance on the gate voltage (see Fig.3).

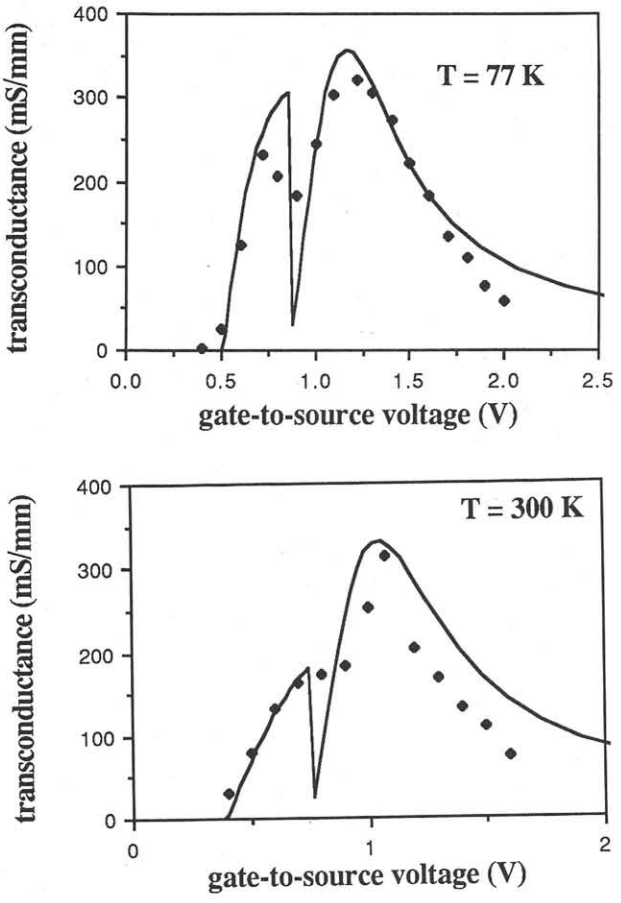

Fig.3 Measured and calculated transconductance of SL-MODFET at 77 K and 300 K.

In all our devices the gate current causes the drop in the transconductance at high gate voltages (2-3V). The maximum transconductance is also limited by the source series resistance. We have developed a model which accounts for the new mechanism of the gate current in our devices and allows us to predict the device current voltage charactristics in good agreement with the experimental data. According to this model the mechanism responsible for the gate current in HIGFETs changes drastically at the gate voltage equal to to the threshold voltage. At the gate voltages below the threshold voltage the gate current is determined by the thermionic emission over the Schottky barrier at high temperatures and by the thermionic-field emission at low temperatures. Above the threshold the gate current is determined by the new mechanism which is the thermionic emission over the conduction band discontinuity at high temperatures and by tunneling through the AlGaAs layer at low temperatures (see Fig.4).

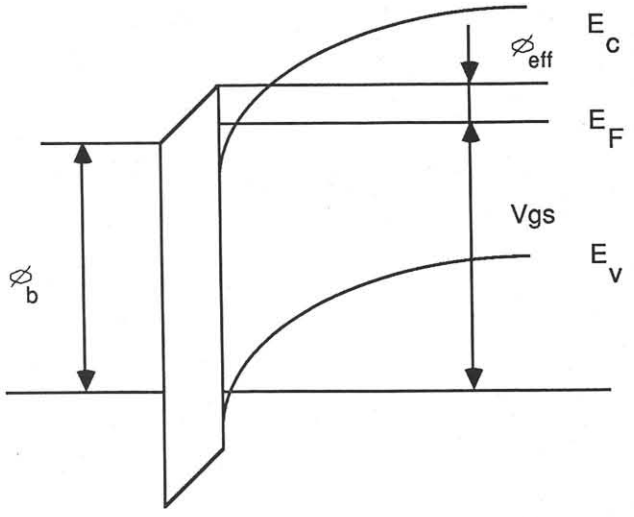

Fig.4. Band diagram of a HIGFET for gate voltages above threshold. As can be seen from the figure the effective barrier height limiting the gate current is determined by the conduction band discontinuity.

As can be seen from Fig.5 our theory is in very good agreement with the measured data.

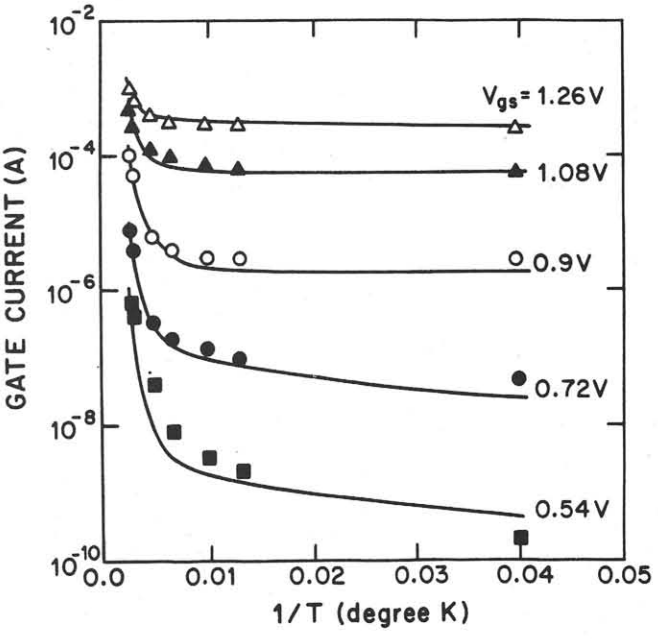

Fig.5. Gate current as a function of T^{-1} for different gate-to-source voltages. Experimental data and calculated curves (solid lines) [10].

We also developed an improved charge control model describing SL-MODFETs and HIGFETs. Some of the results are shown in Fig.6 and 7 where we compare the calculated and measured characteristics of the SL-MODFETs and n and p-channel HIGFETs.

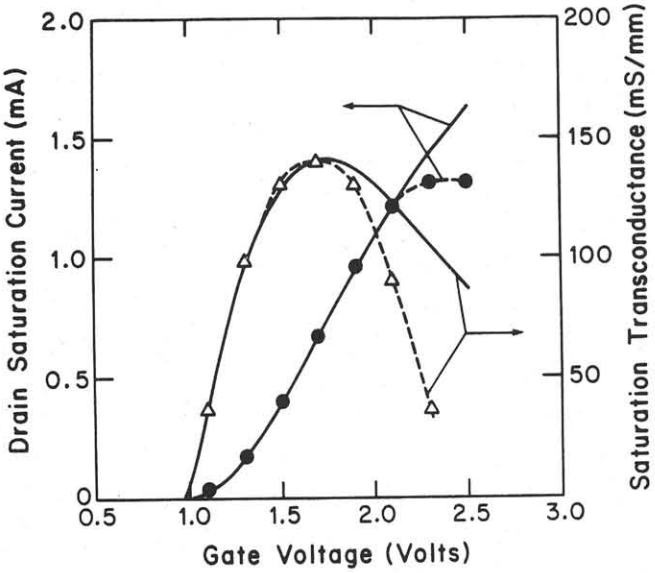

Fig.6. Drain-to-source saturation current and transconductance vs. gate voltage for an n-channel HIGFET [11].

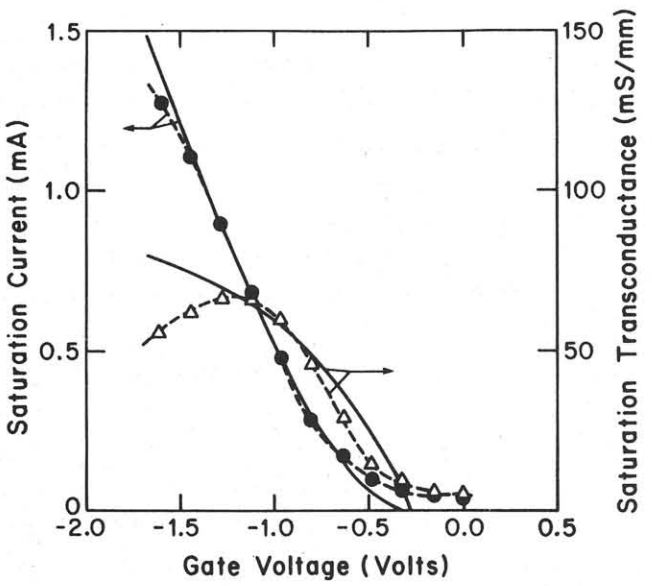

Fig.7. Drain-to-source saturation current and transconductance vs. gate voltage for a p-channel HIGFET [11].

Our model allows us to establish trade-off between charge transfer and gate leakage by changing the gate-to-channel spacing.

We have fabricated digital HIGFET and SL-MODFET ICs and obtained gate propagation delays as short as 22 pS (42 pS for fan-out of 2.5). These results together with small variation of threshold voltage across the wafer, the insensitivity of the device characteristics to light and little dependence of the threshold voltage on temperature indicate a great potential of our technology for ultra-high speed low power applications.

References.

1.N.C.Cirillo,Jr., M.S.Shur, P.J.Vold, J.K.Abrokwah, and O.N.Tufte, IEEE Electron Device Letters, vol.EDL-6, Dec. 1985

2. D.K.Arch, J.K.Abrokwah, P.J.Vold, A.M.Fraasch, R.R.Daniels, M.S.Shur, and J.Xu, Device Research Conference, Amherst, June 1986

3.N.C.Cirillo, Jr., M.S.Shur, and J.K.Abrokwah, IEEE Electron Device Letters, vol.EDL-7, pp.71-74, Feb.1986

4. N.C.Cirillo, M.S.Shur, P.J.Vold, J.K.Abrokwah, R.R.Daniels, and O.N.Tufte,IEDM Technical Digest, 1985, pp.317-320, IEEE, December 1985

5. M.S.Shur, D.K.Arch, R.R.Daniels, and J.K.Abrokwah, IEEE Electron Device Letters, vol.EDL-7, pp.78-80, Feb.1986

6. A.Kastalski and S.Luryi, IEEE Electron Device Letters, EDL-4, 334, 1983

7. A.Kastalski, S.Luryi, A.C.Gossard, and W.K.Chan, IEEE Electron Device Letters, EDL-6, 347, 1985

8.K.Hess, H.Morkoc, H.Shichijo, and B.G.Streetman, Appl.Phys.Lett., 35, 469, 1979

9.M.Keever, H.Shichijo,K.Hess, S.Banerjee, L.Witkowski, H.Morkoc, and B.G.Streetman, Appl. Phys.Lett., 35, 459, 1979

10.J.H.Baek, M.S.Shur, R.R.Daniels, D.K.Arch, J.K.Abrokwah, and O.N.Tufte, New mechanism of the gate current in Heterostructure Insulated Gate Field Effect Transistors, unpublished.

11. J.H.Baek, M.S.Shur, R.R.Daniels, D.K.Arch, J.K.Abrokwah, and O.N.Tufte, Current-voltage and capacitance-voltage characteristics of Heterostructure Insulated Gate Field Effect Transistors, unpublished.