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A Thin AlGaAs Barrier n^+-Ge Gate MISFET with High Transconductance

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Abstract The transconductance dependence on the gate barrier thicknness of n^+-Ge gate MISFET was studied to obtain large transconductance. First, the optimum Al mole fraction of gate barrier layer was studied and found to be 0.45. An extrinsic transconductance of 430 mS/mm and intrinsic transconductance of 700 mS/mm were obtained at room temperature for the 0.8 μm gate-length FET with 10-nm thick AlGaAs. Effects on FET characteristics of the two-dimensional electron gas (2-DEG) finite width were found.

1. Introduction

An n^+-Ge gate MISFET using undoped AlGaAs as a gate barrier has great potential for LSI application due to its small positive threshold voltage (V_{th}) and good V_{th} uniformity[1]. In addition, V_{th} is independent of the AlGaAs thickness, so this device promises to achieve large transconductance with a thin AlGaAs layer without affecting the threshold voltage.

In this report, the dependence of FET characteristics on the gate barrier thickness is discussed. The barrier height and the conduction band discontinuity of AlGaAs/GaAs are also discussed in order to optimize the Al mole fraction of AlGaAs barrier. It is shown that a large transconductance of 430 mS/mm is obtained with a thin gate barrier.

2. Barrier height of indirect bandgap AlGaAs

In order to fully develop MISFETs, the gate current should be considered when decreasing the gate insulator thickness. The gate current of n-channel MISFETs is directly governed by conduction band discontinuity (ΔE_c). Recent investigation[2),3)] on band alignment for the full range of alloy compositon were performed by means of p-SIS (semiconductor/insulator/semiconductor) diodes. The valley in $Al_xGa_{1-x}As$ which determines the barrier height for electrons is not yet clear in the indirect bandgap region (x>0.45). To clarify the current conduction mechanism and optimize the Al mole fraction of gate barrier layer, we directly measured the barrier height and the conduction band discontinuity of indirect bandgap AlGaAs/GaAs hetero-junction using n-SIS diodes .

The SIS structures used to determine the conduction band discontinuity were grown by molecular beam epitaxy. A 200 nm thick n^+-buffer layer, a 500 nm thick n^--GaAs layer, a 50 nm thick undoped AlGaAs barrier layer, and a 300 nm thick n^+-GaAs layer were successively grown on (100) n^+-GaAs substrates. The Al mole fractions (x) were 0.48, 0.62, 1. AuGe/Ni/Ti/Au was then evaporated on the back and front sides, and alloyed to make ohmic contacts. Finally, the SIS diode was completed by mesa isolation defining its area to $9X10^{-5}cm^2$.

I-V measurements were carried out in the temperature range from 80 to 330 K. Figure 1 shows the I-V characteristics of the SIS diodes with $Al_{0.62}Ga_{0.38}As$ barrier. The strong temperature dependence of the currents indicates that the thermionic emission process dominates the current conduction mechanism. Similar I-V characteristics were observed for other samples. Barrier height (ϕ) was determined from the slope of $\ln(J/T^2)$ vs $1/T$. C-V measurements were also carried out at 80 K to determine the parameters of the SIS diodes by fitting the theoretical C-V curve. Flat band shifts were observed for samples

except x=0.48. They are due to the negative charges in nominally undoped AlGaAs. Similar negative charges have been observed in samples from a number of laboratories[3].

Conduction band discontinuities were evaluated using the barrier height data and the SIS diode parameters obtained by C-V measurements. The effects of the negative charges in the AlGaAs layer and the temperature dependence of the Fermi level[3] were taken into account in the analysis. The evaluated conduction band discontinuities are shown in Fig. 2 by open circles. The solid and dashed lines correspond to the conduction band discontinuities of AlGaAs/GaAs heterojunction for Γ and X-valleys of AlGaAs, respectively. They are calculated from the bandgap data[4] under the assumption that the valence band discontinuity is 35 % of total Γ-valley bandgap difference.[5] When the Al mole fraction is larger than the band cross over point, the measured ΔE_c is nearly equal to the difference between the Γ-valley of GaAs and the X-valley of AlGaAs. ΔE_c decreases when increasing the Al mole fraction. Electron transport through the AlGaAs barrier in the indirect bandgap region is determined by the X-valley of AlGaAs for thermionic emission current. It is concluded that the most suitable Al mole fraction for the insulator layer in n-channel MISFETs is about 0.45 which gives the largest barrier height for electrons.

3. FET characteristics

3-1 Fabrication process

A schematic cross section of a fabricated MISFET is shown in fig. 3. An n^+-Ge was used as a gate electrode to obtain a small positive threshold voltage[1]. The structure composed of undoped GaAs, undoped AlGaAs and n^+-Ge were grown by MBE on S.I.LEC GaAs substrate. Based on the above results, Al mole fraction of the gate barrier layer was chosen to be 0.5. The thickness of AlGaAs layer was varied in the range from 5 to 60 nm. The undoped GaAs layer on the AlGaAs was grown to obtain good ohmic contacts and to protect AlGaAs from oxidation.

The fabrication process of the MISFET after MBE growth was as follows. First, a 200 nm WSi_x layer was deposited, then WSi_x and Ge layers were etched by RIE to form a gate. Next, source and drain n^+-regions, self-aligned to the gate, were formed by Si ion implantation (100 keV, $1X10^{14}cm^{-2}$) and successive lamp annealing at 850°C for 4 s. Finally, the source and drain ohmic contacts were formed by evaporating and alloying AuGe/Ni.

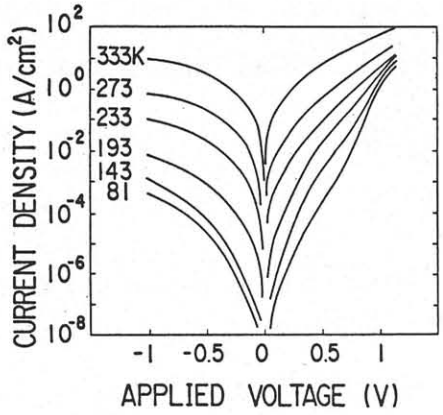

Fig. 1 Temperature dependence of I-V characteristics for the SIS diode with x=0.62 AlGaAs barrier.

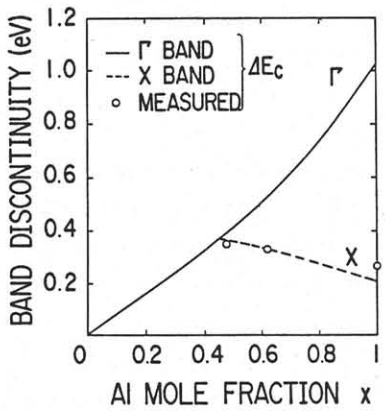

Fig. 2 Conduction band discontinuity as a function of Al mole fraction. The solid and dashed curves corresponds to the Γ and X-valleys of AlGaAs, respectively, assuming the equation $\Delta E_v=0.35\Delta E_{g\Gamma}$.

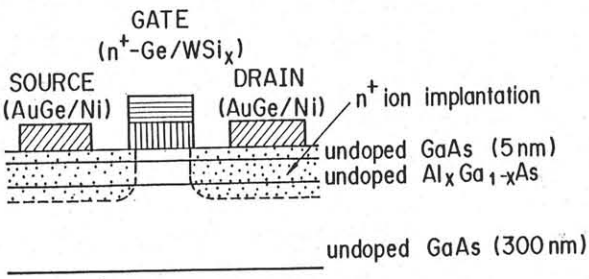

Fig. 3 Schematic cross-section of MISFET.

3-2 Results and discussion

The behavior of FET characteristics for the 3-μm gate-length FET's with various AlGaAs layer thicknesses (d_i) were investigated at room temperature. The variation of the threshold voltage with decreasing AlGaAs layer thickness was less than 0.15 V. Figure 4(a) shows the gate voltage (V_g) dependence of transconductance (g_m). The figure shows that the g_m increases with decreasing AlGaAs layer thickness from 60 to 10 nm. However, a further decrease of AlGaAs layer thickness to 5 nm causes a decrease of the transconductance.

The dependence of gate current (I_g) on gate voltage is shown in Fig. 4(b). The gate current increases with decreasing AlGaAs layer thickness, and it becomes significant for the 5-nm AlGaAs FET. Furthermore, the gate voltage where the transconductance starts to decrease corresponds to the voltage for rapid increase of gate current. Therefore the small transconductance of 5 nm AlGaAs layer FET's and the g_m decrease at high gate voltages are due to the large gate current. The gate current through the source resistance causes the effective gate voltage lowering, resulting in lower transconductance. It should be mentioned that the FET with a 10 nm AlGaAs barrier shows good performance at room temperature in spite of a comparatively small ΔE_c (about 0.35 eV) value. The optimum thickness for obtaining large transconductance is found to be about 10 nm.

Following the simple model of MISFET's, intrinsic transconductance g_{mo} is expected to increase proportionally to the inverse thickness of the insulator layer d_t^{-1}. The thickness d_t is given by the total thickness of the AlGaAs and 5-nm GaAs cap layer. The inverse intrinsic transconductance g_{mo}^{-1} for the 3 μm gate FETs are plotted as a function of d_t in Fig. 5. A small gate bias of 0.2 or 0.3 V from the threshold voltage is chosen to avoid the effect of gate current. The g_{mo}^{-1} curves are linearly dependent on insulator thickness, but they do not cross the origin. This result suggests that the effective insulator thickness is enlarged by Δd, which is given by the x-axis intersection, about 9 nm. This value can not be explained by the depletion layer formation in n^+-Ge, because the impurity concentration in n^+-Ge is as high as $5X10^{19}$ cm^{-3}.

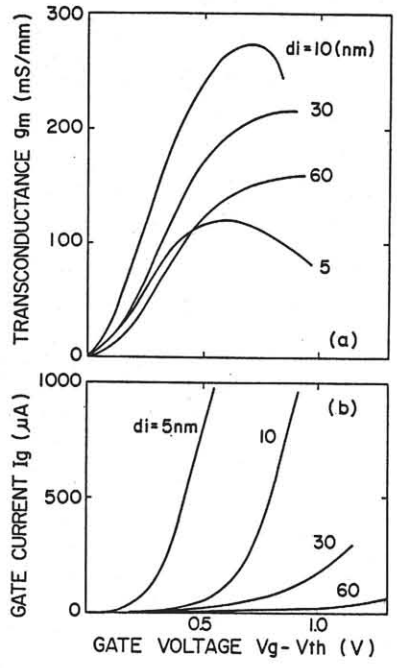

Fig. 4 Dependence of FET characteristics on AlGaAs thickness: (a) transconductance, (b) gate current. The gate length and width are 3 and 20 μm, respectively.

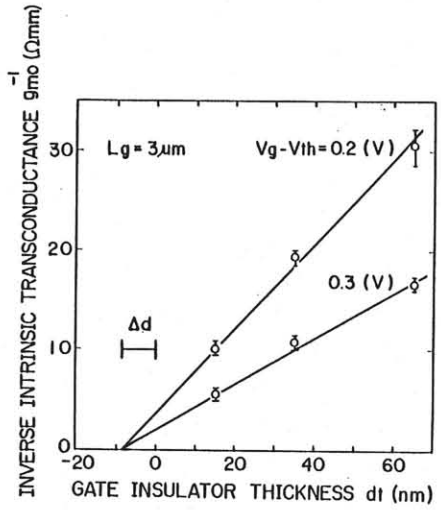

Fig. 5 Dependence of intrinsic transconductance on gate barrier thickness.

This enlarged thickness gives the average distance of the 2-DEG from the AlGaAs/GaAs hetero-interface. The value of Δd obtained in this experiment agrees well with that theoretically predicted by Lee et al.[6]. This is, therefore, the first direct observation of the 2-DEG finite width effect on hetero-junction FET characteristics.

Figure 6 shows the threshold voltage shifts for FET's with 10-nm or 60-nm AlGaAs layer as a function of gate length. The V_{th} shift for 10-nm

AlGaAs layer FETs is much smaller than that for 60-nm AlGaAs layer FETs. This is because reducing the AlGaAs thickness makes the effect of the drain potential on channel small compared with that of the gate potential. Decreasing the gate barrier thickness should play an important role in reducing short channel effects.

The maximum extrinsic transconductance at room temperature is 430 mS/mm for the 0.8 μm gate FET with a 10-nm AlGaAs barrier as shown in Fig. 7. No noticeable influence of gate current on I_D-V_D characteristics are observed for gate voltages up to 1.3 V. The corresponding intrinsic transconductance is about 700 mS/mm. This large transconductance demonstrates the inherent potential of the MISFET for LSI application.

4. Summary

The transconductance dependence on gate barrier thickness was studied in order to obtain large transconductance MISFETs. First, barrier heights and conduction band discontinuities of indirect bandgap AlGaAs/GaAs were investigated using n-SIS diodes to optimize the Al mole fraction of the gate barrier layer. It was found that the X-valley governs the current conduction and hence the most suitable Al mole fraction for n-channel MISFET is about 0.45.

Next, n^+-Ge gate MISFET's with various thickness of AlGaAs layer were fabricated. The optimum thickness of the AlGaAs layer for large transconductance was found to be about 10 nm. It was experimentally verified that the average distance of the 2-DEG from the hetero-interface is about 9 nm. An extrinsic transconductance of 430 mS/mm and intrinsic transconductance of 700 mS/mm were obtained for a 0.8 um gate-length FET with 10-nm thick AlGaAs. Moreover, thin gate barrier FETs were found to be less affected by short channel effects. These results show the effectiveness of decreasing the gate barrier thickness for improving MISFET performance.

Acknowledgment

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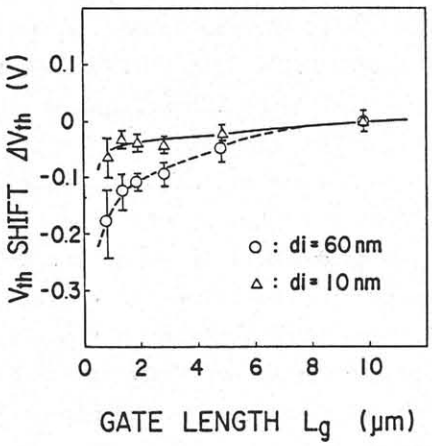

Fig. 6 Threshold voltage shift as a function of gate length.

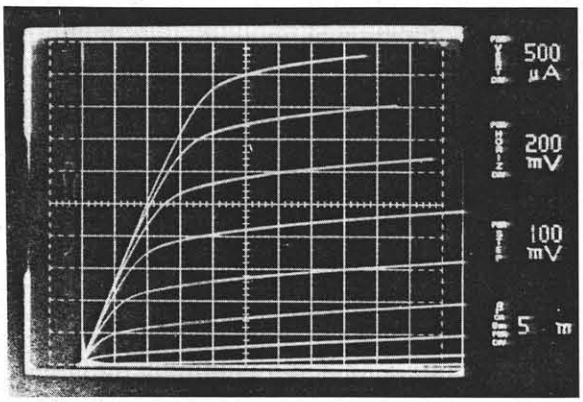

Fig. 7 I_D-V_D characteristics of a MISFET. V_{gmax} is 1.3 V with a 0.1 V step. The gate length and width are 0.8 and 20 μm, respectively.

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