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A Sub-nanosecond GaAs 8b ALU by LSCFL

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A GaAs 8b Arithmetic Logic Unit (ALU) is designed using Low-power Source Coupled FET Logic (LSCFL) and successfully fabricated with 0.5 μm BP-SAINT FETs. An ultra fast operation of 0.8 ns critical path delay time is obtained, equivallently corresponding to a loaded delay time of 57 ps, which is the highest speed achieved in an LSI thus far.

INTRODUCTION

GaAs digital LSIs have been developed actively to satisfy demands for giga-bit rate communication systems and high speed computers. In 1984, 16 Kb static RAM(1) integrating over 100,000 devices was successfully fabricated to demonstrate GaAs VLSI feasibility. As for logic LSIs, a full-custom designed 16x16-bit parallel multiplier(2), a 2K gate array using DCFL(3) and a 3K gate array using BFL(4) have been reported. Unloaded gate delay time (t_{pd0}) obtained with ring oscillator TEGs in these logic LSIs are 30-50 ps, however, loaded gate delay times (t_{pdL}) are 100-150 ps for the full-custom logics and 150-250 ps for the gate arrays. These t_{pdL}s are comparable to that of the best Si bipolar LSI(5). In order to achieve higher GaAs LSI speed, it is necessary to improve GaAs MESFET characteristics by increasing transconductance (g_m) and by reducing the gate capacitance (C_{gs}), and also to refine the basic circuit applied for LSIs.

This paper describes the design and fabrication results of a GaAs 8b ALU LSI. The high speed and low power performances of LSCFL have been demonstrated in sequential logics such as a 11 GHz frequency divider(6) and a 2 Gb/s digital time switch LSI(7). Here, LSCFL is adopted to construct various functional gates with series gate implementation for combinatorial logic design of the ALU LSI. The most effective way to improve FET characteristics is to reduce gate length without the short channel effects. 0.5 μm gate BP-SAINT(8) is sucessfully applied to the LSI. An ultra-fast operation of 0.8 ns critical path delay time is obtained with the LSI, which equivallently corresponds to the loaded delay time of 57 ps, and it is the highest gate speed achieved in LSIs thus far.

DESIGN

The designed 8b ALU consists of two 4b ALU blocks connected by a ripple carry, as shown in Fig.1. The ALU has 16 arithmetic functions and 16 logical functions, the same as standard ECL logic families (ECL-10K). In Fig.1, M is mode control, S0-S3 are function select inputs, A0-A7 and B0-B7 are operand inputs, C_n is a carry-in, F0-F7 are function outputs, and C_{n+4} is a carry-out. (C_{n+4}) is a carry-out of the left side lower 4b block and is connected to (C_n), which is a carry-in of the right side higher 4b block.

An advanced design approach utilizing the 3-level series gate LSCFL is used as the basic circuit of the ALU LSI. Series gate LSCFL features are : (1) high speed due to true and complementary inputs and outputs, (2) low power dissipation by enhancement FET implementation,

(3) wide acceptable V_{th} range of $-0.25\ V < V_{th} < 0.3\ V$, and (4) functional gate availability. LSCFL was confirmed to have a higher speed than DCFL in sequential logic used in the time switch LSIs[7,9] mainly composed of flip-flops(F/F). In this work, the applicability of LSCFL to combinatorial logic like ALU, where logic gates are mainly used, is investigated. Series gate level number is optimized at three, considering logic function flexibility, speed, and power dissipation. Series gate configuration is useful for realizing a complex logic function by a unit gate, and reducing passage gate number. For example, in a master-slave DFF, the passage gate number is 4 with DCFL in which only a NOR gate is available, but it is 2 with LSCFL. Therefore, LSCFL DFF has nearly twice the toggle frequency of DCFL.

Typical circuit configuration with a three level series gate is a 3-input exclusive OR/NOR circuit applied to the ALU, as shown in Fig.2. To realize this function, only $1 \cdot t_{pd}$ is needed by LSCFL, as compared to $3 \cdot t_{pd}$ for DCFL. However, in a gate with a simple function like OR/NOR, series gate LSCFL has no advantage over DCFL from the viewpoint of speed performance. The internal passage gate number of the 8b ALU critical path without I/O buffers can be reduced to 8 by logic optimization. This is 2/3 that of the DCFL ALU's 12. Consequently, the average logic ability of LSCFL is 1.5 times higher than NOR gates in a combinatorial logic. The t_{pd} of the series gate has been found by circuit simulation to depend on the input level: the lower, the input level, the greater the t_{pd}. By the measurements of various LSCFL functional gate ring oscillators fabricated on the same wafer as the ALU, this tendency is confirmed as shown in Fig.3. The average unloaded inverter delay time (t_{pd0}) is 35 ps (Fig.3). In the figure, the functional gate t_{pd} is found to depend on the input-output level, and t_{pd} of level-3 (a_3) is twice as large as level-1 (c_1). Considering this effect, a critical input is connected to level-1 in OR/NOR and exclusive-OR/NOR where three kinds of inputs are logically exchangeable, in order to achieve the highest possible speed. The standard cell approach is adopted for the layout design, and 5 kinds of cells and their power cells are used

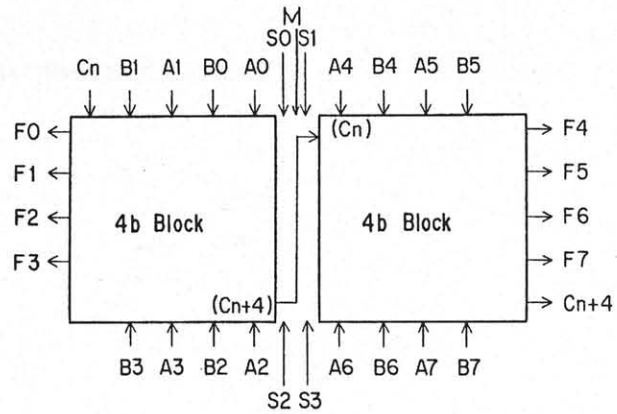

Fig.1 Block diagram of GaAs 8b ALU.

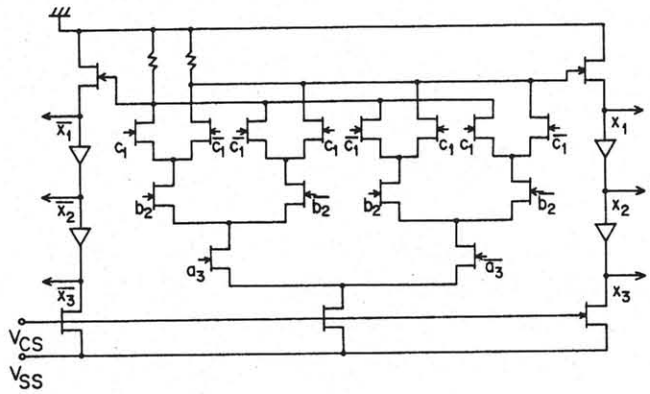

Fig.2 3-input exclusive OR/NOR circuit by LSCFL.
$X = a \oplus b \oplus c$

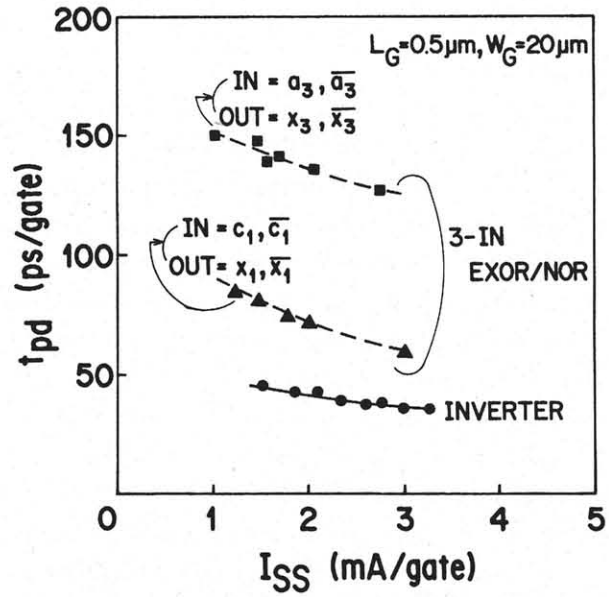

Fig.3 Propagation delay times of LSCFL ring oscillators versus supply current.

depending on load conditions.

Enhancement FETs with 20 μm gate width are mainly used for both switching FETs and source follower FETs and diodes. Designed supply voltages are -3.5 V for Vss and 0.6 V for Vcs. Both input and output levels are designed to be ECL compatible using internally generated reference voltage Vref = -1.3 V in input buffers. 400 μm gate wide E-FETs are used in the open-drain type output buffers.

FABRICATION PROCESS

Fabrication technology is 0.5 μm-gate BP-SAINT. 30 keV ion implantation energy is adopted to form a shallow active layer. The technique of parallel ion implantation into 3-inch low dislocation desity crystal is newly developed to improve uniformity and reproducibility. Owing to the buried p-layer and shallow active layer, the short channel effect is effectively suppressed, as shown in Fig.4. As a result, a gate length of 0.5 μm can be applied for the LSI fabrication. The average V_{th} and g_m are 0.04 V and 230 mS/mm, respectively. The airgap process is effectively adopted to reduce interconnect capacitances. A microphotograph of a fabricated 8b ALU is shown in Fig.5. Chip size is 3.34 mm x 2.52 mm. The LSI consists of 1426 elements (FETs, diodes, and resistors), and contains an equivalent of 250 gates.

MEASURED RESULTS

Add (M=0, S=0110) and Subtract (M=0, S=1001) mode function tests were carried out, and all paths in the LSI are confirmed to operate correctly. Propagation delay times are measured for F0, F2, F4, F6 and C_{n+4} in Add mode by using an on-wafer high frequency probe card. The measurement result of critical path delay time from A2 to F6 is 0.9 ns before the airgap process and afterwards, it is improved to 0.8 ns, as shown in Fig.6. The test pattern applied here is A=(00000X00), B=(11111111) and C_n=0 in the Add mode. The obtained critical path delay times of 0.8 ns with airgap and 0.9 ns without airgap coincide with the simulated results, including actual fan-out and line capacitance estimated

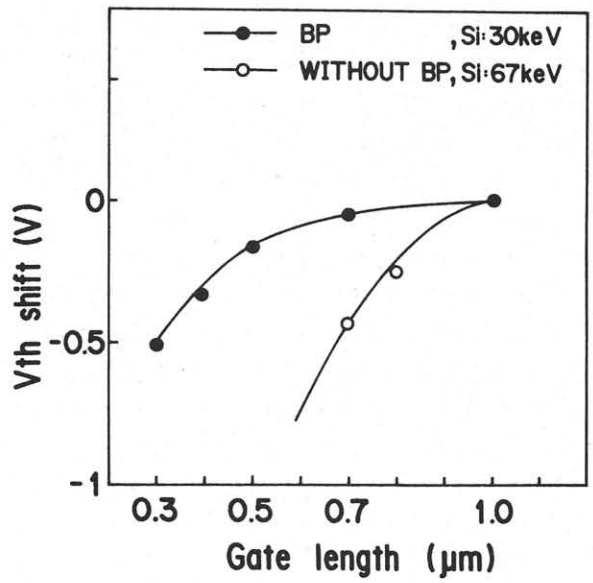

Fig.4 Threshold voltage shift dependency on gate length.

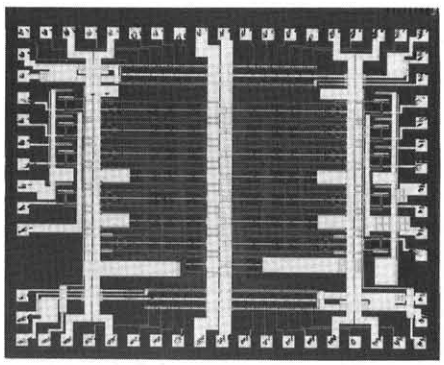

Fig.5 Microphotograph of a fabricated GaAs 8b ALU. Chip size is 3.34 mm x 2.52 mm.

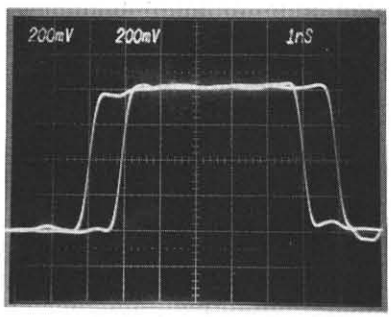

Fig.6 Delay time measurement result from A2 to F6 in Add mode. Delay time is 0.8 ns.

from the layout pattern. An output signal swing of 0.8 V into a 50 ohm load is also confirmed (Fig.6). Power dissipations are 1420 mW for the internal gates, 200 mW for the input buffers, 544 mW for the output buffers, and 2.16 W in total.

The average internal LSCFL functional gate delay time with an average Fan Out of 2 and interconnect length of 0.95 mm is obtained to be 80 ps, from the critical path passage gate number of 10 including input and output buffers. However, the equivalent critical path gate number is calculated to be 14 in terms of NOR gates, so that the equivallent gate delay time is estimated to be 57 ps with 5.7 mW/gate. It is found that 57 ps is the best loaded gate delay time (t_{pdL}) in LSIs. The relationship of t_{pdL} to t_{pd0} is shown in Fig.7. The ratio between t_{pdL} and t_{pd0} is decreased to less than two by this design, which is half that of the DCFL LSI fabricated by a similar LSI process.

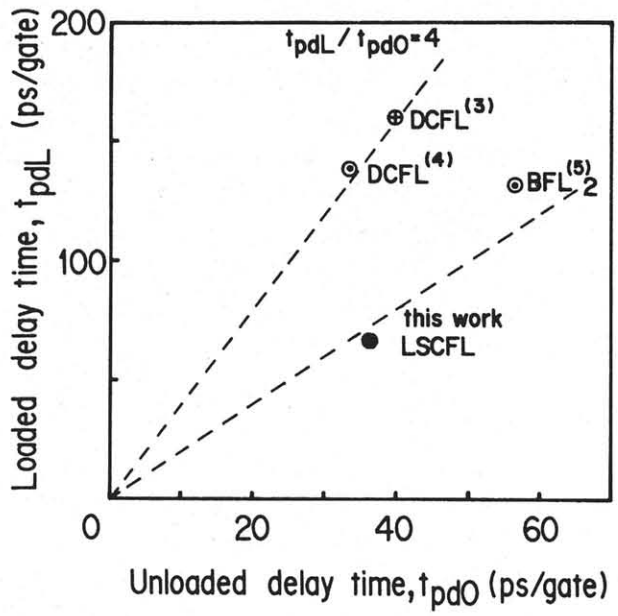

Fig.7 Relationship between loaded delay time (t_{pdL}) and unloaded delay time (t_{pd0}).

CONCLUSION

A GaAs 8b ALU is designed by using 3-level series gate LSCFL and fabricated by adopting 0.5 um-gate BP-SAINT FETs. A very high speed operation of 0.8 ns critical path delay time and an equivallent loaded gate delay time of 57 ps, the highest speed ever reportedin an LSI, are obtained. By this result, the feasibility of an ultra high speed GaAs logic LSI is demonstrated.

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