An SLCF Circuit: A Large Noise Margin, High-Speed and Moderate Power Dissipation Circuit for Reliable GaAs LSI Operation

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A new GaAs logic circuitry, named "Schottky diode Level shifter Capacitor coupled FET logic (SLCF)" has been developed. It has driver DFETs and a load DFET in the logic stage, in front of which a level shifting stage including a Schottky diode is connected. The main feature of the circuit is that the Schottky diode performs level shifting as well as feed-forward capacitor coupling of the input signal. It offers high-speed, 40 ps/gate, and a larger noise margin than DCFL, with around 1 mW/gate power consumption, which ensures reliable and stable GaAs LSI operation with 4K-8K gate complexity.

1. Introduction

Recently, high-speed GaAs logic LSIs with 1-3K gates have been developed.1,2 In these GaAs LSIs, there are two circuit implementation categories. One uses only depletion mode MESFETs (DFETs) and the other uses enhancement mode MESFETs (EFETs). Direct Coupled FET Logic (DCFL) is a typical EFET logic and is characterized as a low power and high-speed circuit. On the contrary, DFET logic, such as Buffered FET logic (BFL) and Schottky Diode FET Logic (SDFL), consumes more power in its complicated gate structure. However, it has the advantage that it has a larger noise margin. When a GaAs LSI is designed, the power limit in a chip has to be carefully considered, and a logic circuitry with low power and compact layout is strongly desired. From this viewpoint, DCFL is most promising. However, another circuit aspect is that an adequate noise margin is necessary for reliable LSI operation. DCFL shows only a 0.2V noise margin at the most. Therefore, it requires tight FET threshold voltage control and a low sheet resistivity metal layer to minimize power line voltage drop which worsens the noise margin. In this respect, when complexity reaches more than several thousand gates in a chip, DCFL becomes less attractive, based on the present GaAs process technology status.

This paper proposes a new logic circuitry for 4-8K GaAs LSIs with a large noise margin, high-speed and moderate power dissipation performance. This new logic consists of DMESFETs, and a diode which operates as a level-shifter and a feed-forward capacitor as well. Therefore, this new circuitry has been named "Schottky diode Level shifter Capacitor coupled FET logic (SLCF)". After describing the basic operation of this new logic circuitry, DC and AC performances will be described.

2. SLCF gate design

A circuit diagram for a 2-input NOR gate is shown in Fig.1. Two power supplies are required, 1.5 V and -1.0 V. In this gate, the logical NOR function is provided by two driver DFETs, Q2 and Q2', which have different threshold voltage from the load DFET Q1 in order to achieve a better noise margin. Schottky diodes D1 and D1' provide the level shifting required between output at the drain and input at the gate electrode of the

![Fig.1 2-input NOR gate implemented by SLCF circuitry.](image-url)
driver DFET. Therefore, operation at the DC mode resembles an SDFL gate, resulting in almost twice larger noise margin than for a DCFL. What is different from an SDFL is that these Schottky diodes act as a feed-forward capacitor like a capacitor in a CDPL and FFS to obtain higher speed performance with less power dissipation. Pull-down FETs, Q3 and Q3', provide the bias current for the diodes for adequate level shifting, and the current is designed to be one-tenth of the load current for Q1. Therefore, the fan-out characteristic for SLCF gate is 2–3 times superior to that of SDFL gate.

Special care should be taken to let the diode operate for both level-shifting and capacitor coupling. The diode is designed with the following attention. First, the capacitance of the Schottky diode should be at least twice as much as the gate-to-source capacitance for the driver FET, to avoid reduction of the signal amplitude due to charge sharing at the AC mode. The recommended multiplying factor C/D1/CQ2, which is used under standard conditions, is 4–6, considering speed and layout area trade-off. Differing from CDPL and FFS, which have a large coupling capacitor at the output side in addition to level shifting diodes, the SLCF has a diode acting as a level shifter and a coupling capacitor at the input side, resulting in much smaller required capacitance and thus a very small diode area. Therefore, its layout compactness is superior to CDPL and FFS. Second, the Schottky diode should be heavily and deeply doped to avoid rapid reduction in capacitance by the pinch-off mechanism.

The SLCF has another merit; it is possible to realize a 2-input NAND gate, which is constructed with two driver FETs, Q2 and Q2', in series.

3. Circuit fabrication

SLCF circuits were fabricated by the WN$_x$ self-aligned gate process. FET channel layers were formed by $^{28}$Si$^+$ ion implantation into a GaAs semi-insulating 3-inch diameter LEC wafer, followed by a capless annealing process. Source and drain n$^+$ regions were also formed by $^{28}$Si$^+$ heavy dose implant. The Schottky diode was made by WN$_x$ deposited on a GaAs n-layer, which was formed by simultaneous implanting with channel formation to be undepleted under any operating bias condition. Table 1 summarizes the gate width and length of Q1-Q3 and D1 shown in Fig.1 as standard conditions. Table 1 also shows the properties of the obtained MESFETs Q1-Q3 and diode D1. Two kinds of SLCF were examined, one had a nominal gate length $L_g$ of 1.5 µm (type 1), and the other had 1.2 µm (type 2). The former was used to examine the basic SLCF gate operation, and the latter was used to obtain higher gate performance, especially speed performance. Figure 2 is a photomicrograph showing one stage of a ring-oscillator (type 1). The SLCF gate was constructed using a diode, a load FET and a driver FET. The SLCF gate capacitor diode size was 60 µm$^2$, which was much smaller than coupling capacitor sizes in other DFET logics, like CDPL and FFS.

4. SLCF gate performance

Figure 3 shows simulated and measured DC

| Table 1 Properties and device sizes used in standard SLCF gate. |
|-----------------|-----------------|-----------------|-----------------|
| FET             | W/L (µm)        | Vth (V)         | K-value (mA/µm$^2$) | V pinch-off (V) |
| Q1              | 10/1.5          | -0.600          | 1.11              | -----          |
| Q2              | 10/1.5          | -0.398          | 1.24              | -----          |
| Q3              | 2/3             | -0.620          | 0.131             | -----          |
| D1              | 10/6            | -----           | -----             | -2.5           |

| FET             | W/L (µm)        | Vth (V)         | K-value (mA/µm$^2$) | V pinch-off (V) |
| Q1              | 10/1.2          | -0.624          | 1.24              | -----          |
| Q2              | 10/1.2          | -0.422          | 1.38              | -----          |
| Q3              | 2/2.75          | -0.603          | 0.141             | -----          |
| D1              | 10/6            | -----           | -----             | -2.5           |

Fig.2 SLCF gate photomicrograph.
transfer characteristics for the inverter gate with one fan-out and the 2-input NAND gate with one fan-out using two driver DFETs in series. Threshold voltages for Q1 and Q2 (Q2') were -0.355V and -0.255V, respectively. From these results, the following values could be obtained. The inverter gate noise margin values for logic "0" input and logic "1" input were 0.34V and 0.47V, respectively. Values for the NAND gate were 0.22V and 0.47V, respectively. The inverter and NAND gate logic swings were 1.01V and 0.91V, respectively. The inverter and NAND gate transfer gains were 5.48 and 5.35, respectively. Simulation was carried out by using SPICE JFET model. The simulated values agree fairly well with the measured results. This means that noise margin analysis can be performed by means of SPICE circuit simulation, in spite that the above transfer curve evaluation was carried out for different FET parameters from those presented in Table 1.

The simulated noise margin dependence for an SLCF gate on the threshold voltage for load FET Q1 and driver FET Q2 (V_{TD1} and V_{TD2}) is shown in Fig.4. The DCFL noise margin dependence is also shown for comparison. The simulated noise margin in Fig.4 does not coincide with the measured one shown in Fig.3. This is because the measured one is based on the FET with an unintentionally obtained low Schottky barrier height, and high drain conductance. However it does not make the analysis shown in Fig.4 invalid. Figure 4 indicates that the noise margin for a DCFL gate is twice superior to that for DCFL, resulting in better reproducibility and higher yield than when choosing a DCFL.

Before examining the SLCF loaded AC performance, the feed-forward effect of the diode capacitance was investigated by varying the coupling capacitor by means of changing diode sizes. Unloaded ring-oscillators were fabricated to examine the effect. The measured results are shown in Fig.5. It was found that the propagation delay time, t_{pd}, increased with decreasing diode size. This means that the feed-forward effect contributes to the improvement of speed performance. When the diode size reached more than 60 μm², which was more than 4 times larger than the size of the driver FET Q2, t_{pd} became almost constant.

To measure the t_{pd} dependence on load capacitance, two kinds of 15-stage ring-oscillators with different load capacitance at each stage were prepared. The capacitance values were 105 fF and 460 fF. Figure 6 shows the measured results. The plotted data are the average values. Broken lines show simulated results for an SLCF, DCFL and SDFL gate. For below 200 fF load capacitance, t_{pd} for SLCF was superior to that for SDFL because of the feed-forward effect. Incremental delay times for various load conditions were evaluated at P_d=0.96 mW/gate power dissipation; They were 10 ps/fan-in, 55 ps/fan-out and 0.67 ps/fF capacitance. The load drivability for SLCF is almost the same as for DCFL, when P_d=0.96 mW/gate for SLCF and 0.3 mW/gate for DCFL.

In order to achieve higher speed performance, FETs with 1.2 μm gate length were used (type 2). Figure 7 shows the measured results of t_{pd} plots as a function of supply voltage V_{dd} and V_{as}. Broken lines stand for the
simulated results. As supply voltage $V_{dd}$ changed from -1V to -3V, $t_{pd}$ for SLCF was almost constant. However, $t_{pd}$ decreased as the supply voltage $V_{dd}$ increased from 1.5V to 3V. Compared to the speed performance for type 1 (70 ps/gate at 0.96 mW), $t_{pd}$ for type 2 reaches 40 ps/gate at 1.2 mW/gate ($V_{dd} = 1.5V$) and 29 ps/gate at 4.0 mW/gate ($V_{dd} = 3.0V$). These characteristics mean that the circuit can guarantee a reliable and stable operation for 4K-8K gate level LSIs without sacrificing the speed advantage of a GaAs circuit.

5. Conclusions
A new GaAs logic circuitry, named "Schottky diode Level shifter Capacitor coupled FET logic (SLCF)", has been developed. The SLCF circuit has a twice larger noise margin than DCFL and its layout compactness is relatively good, in spite of using a feed-forward capacitor.

A 40 ps/gate speed performance was achieved using FETs of 1.2 µm gate length at $P_{d}=1.2$ mW/gate, which is a higher performance compared to other DFET logics. In addition, it offers moderate power dissipation of around 1 mW/gate region, which is acceptable for 4K-8K gate complexity LSIs. The feed-forward capacitor effect was also described. The multiplying factor of $C_{p1}/C_{Q2} = 4-6$ was the best, considering speed performance and layout area trade-off. SLCF gate load drivability was almost the same as for DCFL.

The above results show that the SLCF circuit has advantages for application to GaAs LSIs ranging in complexity from 4K to 8K gates.

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Fig.5 Relation between propagation delay time and diode area.

Fig.6 Propagation delay time dependence on load capacitances.

Fig.7 Speed-power product as a function of supply voltages $V_{dd}$ and $V_{ss}$. 378