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A 15 GHz Dynamic Binary Frequency Divider Fabricated by GaAs ADVANCED SAINT with Asymmetric N^+-Layers

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(ABSTRACT)

Ultra-high speed ICs are required in satellite communication and microwave communication systems etc.. An ADVANCED SAINT structure with asymmetric source and drain n^+-layers was studied to fabricate 0.3 μm gate-length FETs without short channel effects in order to realize ultra-high speed ICs. BFL dynamic binary frequency dividers fabricated with ADVANCED SAINT operated up to 15.2 GHz.

In conventional BP(Buried P-layer)-SAINT structure[1], the spaces between gate and n^+-layers are fixed at 0.2~0.25 μm to reduce source series resistance. So, the short channel effects are striking at the 0.3 μm gate-length, because the space between n^+-layers(L_n+) decreases less than 1 μm. To overcome these disadvantages, L_n+ was fixed at 1.0 μm, and the spaces between the source n^+-layer and the gate, between the drain n^+-layer and the gate were designed to be 0.25 and 0.45 μm, respectively (Fig. 1(a)). This asymmetric n^+-layer structure was fabricated by self-alignment technology, that is, the oblique ion-implantation with a T-shaped resist mask(Fig. 2(b)). Moreover, the gate electrode was formed by self-alignment technology on the schottky contact region to reduce parasitic capacitances[2].

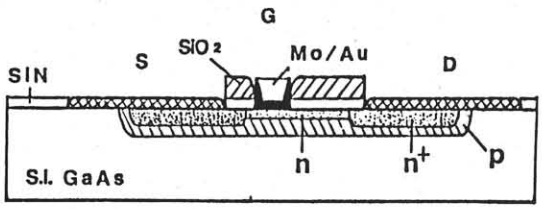
Table 1 summarizes average DC characteristics of ADVANCED SAINT FETs with 0.3 μm gate-length in 3-inch wafer. An increase in short channel effects was not observed.

ADVANCED SAINT FETs with 0.3 μm gate-length were applied to BFL dynamic binary frequency dividers[3]. Figure 2 shows a microphotograph of the frequency divider. Chip size is 1x1.1 mm^2. Input pads(CK,$\overline{CK}$) and output pad(Q) are connected to transfergate FETs and the buffer, respectively, with coplanar 50 ohm lines. The input signal was monitored by MCK or $\overline{MCK}$ pads. Measurements are carried out on wafer by using the high frequency probes. The loss of the measurement system is less than 8 dB up to 18 GHz. A maximum toggle frequency of 15.2 GHz, the highest frequency in any semiconductor devices, was obtained. Figure 3 shows the operating waveforms at 15.0 GHz with power dissipation of 673 mW. Frequency dependences of input sensitivity and output amplitude with 50 ohm loads are shown in Fig. 4. The highly sensitive region was 9.5~14.5 GHz.

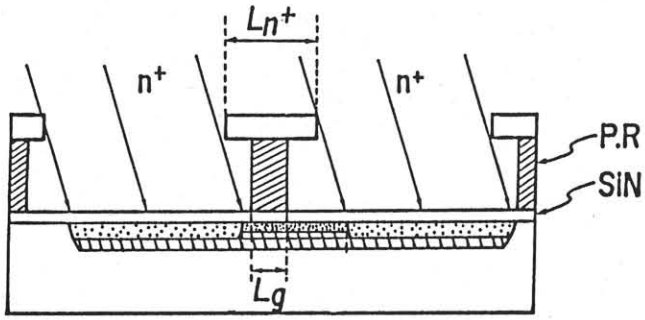
In conclusion, frequency divider operation above 15 GHz has been achieved with ADVANCED SAINT, which is advantageous in shortening gate-length and fabricating ultra-high speed GaAs ICs.

(REFERENCES)

1) K. Yamasaki et al.: Electron. Lett., 20,(1984), pp.1029-1031.
2) T. Enoki et al.: Extended Abstract of the 17th Conference on Solid State Devices and Materials,(1985),pp.413-416.
3) T. Sugeta et al: 1985 ISSCC Digest of Technical Papers, pp.198-199.



(a) Schematic cross-sectional view



(b) T-shape resist and oblique ion-implantation.

Fig.1. Advanced SAINT.

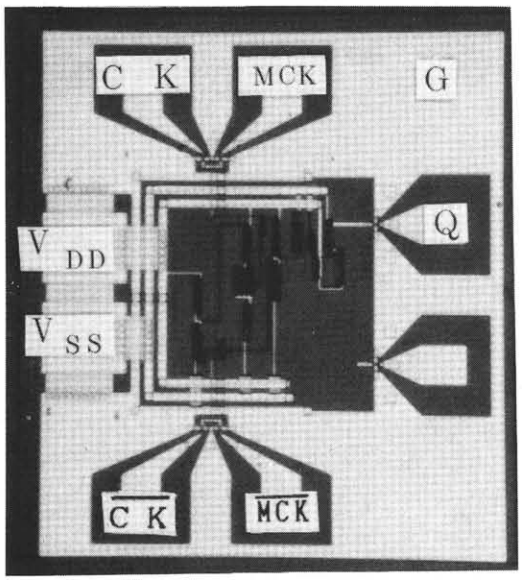


Fig.2. Microphotograph of BFL dynamic binary frequency divider. Chip size is 1x1.1 mm^2

Table 1 Average DC characteristics in 3-inch wafer.

L_g	0.3 μm
V_{th}	-1.22±0.09 V
g_m (V_g= 0 V)	228±19 mS/mm
g_d (V_g= 0 V)	15±2 mS/mm
R_s	0.55±0.08 Ωmm

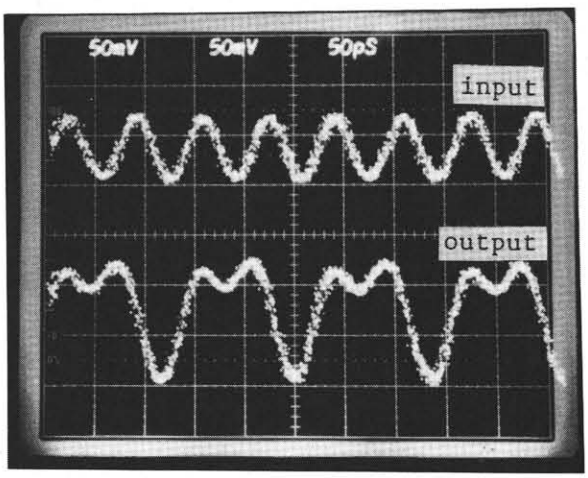


Fig.3. Operating waveform at 15.0 GHz with power dissipation of 673 mW. $V_{in(p-p)}$=1.08V, $V_{out(p-p)}$=163mV with 50 ohm load. V_{DD}= 4.75 V, V_{SS}= -4.5 V.

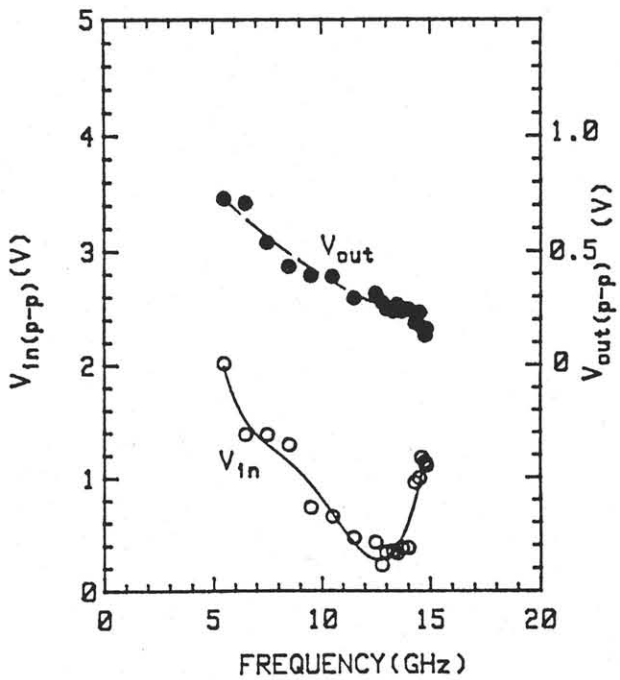


Fig.4. Frequency dependences of input sensitivity and output amplitude. V_{DD}= 4.75 V, V_{SS}= -4.5 V.