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A GaAs Monolithic Operational Amplifier

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ABSTRACT

We demonstrate a GaAs monolithic operational amplifier having such performance as a unity-gain frequency of 200 MHz, an open loop gain of 40 dB, a slew rate of 200 V/μs and a phase margin of 57° for the chip with an FET-geometry of 1μm gate length.

The circuit configuration of the operational amplifier is shown in Fig.1, where the balanced circuit is made up of cascade-connected two differential amplifiers consisting of modified source coupled FET logic (SCFL) inverters (1). This SCFL configuration allows wider distribution in the threshold voltage of the constituent FET's than any other configurations. It is noted that the second differential amplifier is designed using dual-gate FET's so as to achieve an improved frequency response. The frequency compensation circuit, consisting of series resistor and capacitor, is also integrated.

The new ion implantation process (2) is used to obtain high transconductances in the low drain current region, which are essential for the high gain amplifier with high impedance loads. This process, of which implantation steps are shown in Fig.2, realizes a steep tail for the n-layer and a high surface concentration for the n^+-layer by making use of the low voltage n-implantation and the through-oxide shallow n^+-implantation. A photograph of the processed chip is shown in Fig.3. The chip size measures 0.93x1.18 mm^2.

The frequency response of the fabricated operational amplifier is shown in Fig.4. A unity-gain frequency of 200 MHz obtained is more than 10 times higher than those of Si monolithic operational amplifiers. A large phase margin of 57° means that the present amplifier is stable enough even under the full-feedback condition with unity closed loop gain. In Fig. 5, is shown the step response under the full-feedback configuration. The other performance of the present amplifier is summarized in Table I.

References

(1) S.Katsu et al., "A Source Coupled FET Logic—A New current-mode Approach to GaAs Logics", IEEE Trans. Electron Devices ED-32 no.6, pp. 1114-1118, Jun.1985.
(2) I.Ohta et al.,"An Ideal-Profile Implantation Process for GaAs Analog MMICs", Technical Digest, 1986 IEEE GaAs IC Symp. Accepted.

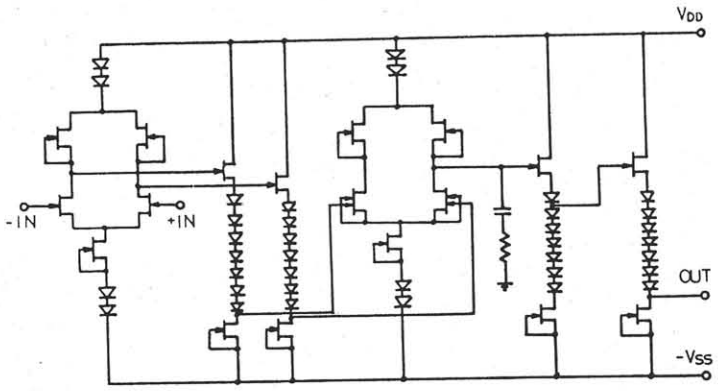

Fig.1. Operational amplifier circuit diagram.

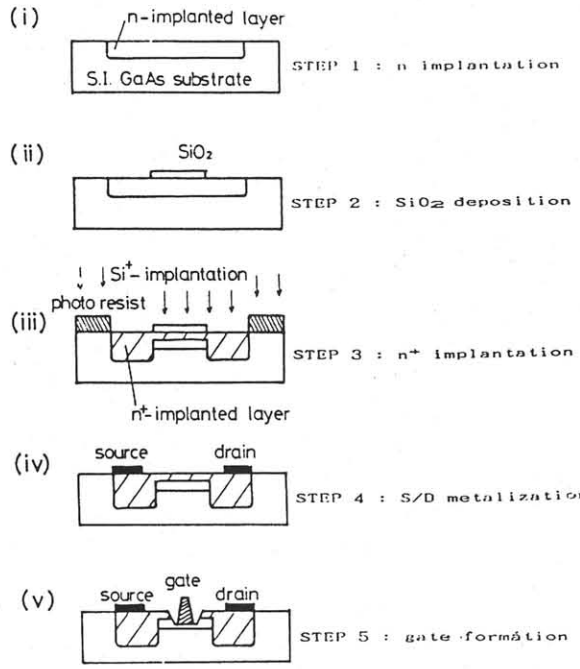

Fig.2. New ion implantation process.

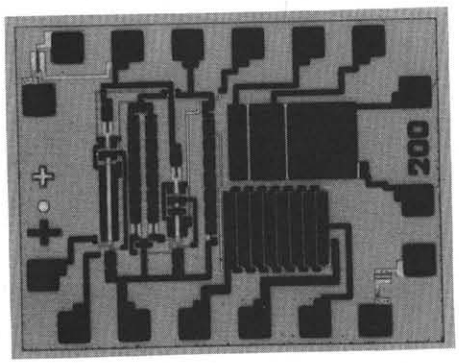

Fig.3. Photograph of the operational amplifier IC.

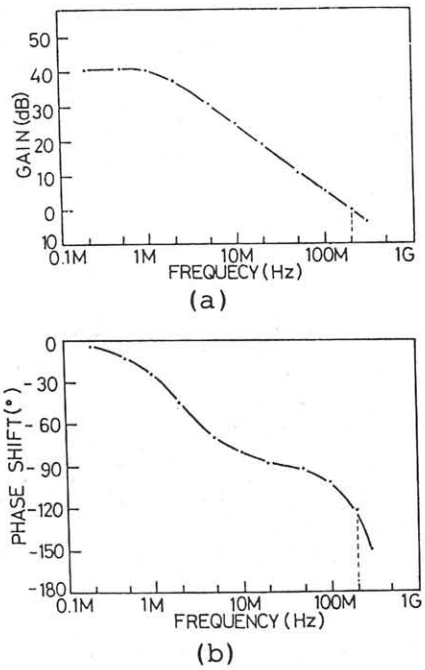

Fig.4. Frequency response of the operational amplifier. (a) Gain. (b) Phase shift.

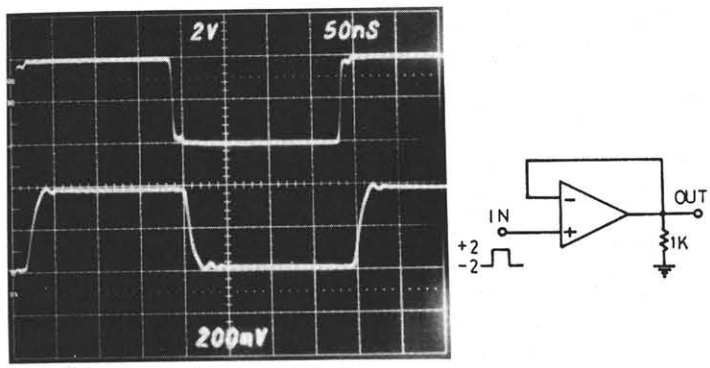

Fig.5. Measured volatage-follower response.

Table I
Performance of the operational amplifier IC.

Unity-gain frequency	200 MHz
Phase margin	57 deg
Slew rate	200 V/μs
Open loop gain	40 dB
Common mode range	+2,-2 V
Power supplies	+12,-3 V
Power supply current	15 mA