Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 379-382

A GaAs Advanced SAINT-FET with Asymmetric N^+ Layers and Its Application to a 20GHz Band Five-stage Monolithic Low Noise Amplifier

M. MURAGUCHI, T. ENOKI, K. YAMASAKI, and K. OHWADA

NTT Electrical Communications Laboratories

3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa Pref., 243-01 Japan

Improvements in RF performance of Advanced SAINT-FETs are described. The asymmetric n^+ layer FET structure is adopted to reduce drain conductance and gate-drain capacitance. The f_{max} of the FET increases 20% due to the improvement. Next, a five-stage monolithic low noise amplifier is fabricated using this processing technology. The amplifier has a measured gain of 13 dB with a noise figure of 7.5 dB around 24 GHz. This is the first five-stage monolithic amplifier which operates successfully above 20 GHz.

1. Introduction

Recent ion implantation technology in the GaAs FET process enables reproducible fabrication of high performance low noise GaAs FETs[1],[2] and monolithic amplifiers[3],[4]. Superior advantages of this technology include economy and the ability to fabricate planar structures for monolithic microwave integrated circuits (MMICs). Self-Aligned Implantation for N^+-layer Technology (SAINT) is one of the most promising process technologies in digital GaAs ICs such as 16Kbit SRAMs[5], 10GHz frequency dividers[6], and 2Gbit/s time switches[7], which also have many advantages in MMICs.

This paper describes improvements in RF performance of a flat-gate SAINT-FET[8] and its application to a 20 GHz band five-stage monolithic low noise amplifier. An asymmetric n^+ layer FET structure is adopted to reduce drain conductance (g_d) and gate-drain capacitance (C_{gd}) without reducing transconductance (g_m) or increasing source resistance (Rs). Here, g_d and C_{gd} as well as g_m and Rs are very important FET parameters in determining gain performance above 20 GHz. Also, the first five-stage monolithic amplifier to operate successfully above 20 GHz is developed. Previously, only two-stage monolithic amplifiers have been reported[3],[4]. The fabricated amplifier has a measured gain of 13 dB with a noise figure of 7.5 dB around 24 GHz.

2. Advanced SAINT-FETs for a Monolithic LNA

(a) FET structure

It is effective to shorten gate length to improve ultrahigh frequency FET performance. However, short-channel effects generally arise when the source-drain distance is shortened with the gate length reductions. As a result, the FET drain conductance increases as source-drain leakage current increases. Drain conductance degrades gain performance in ultrahigh frequencies because it acts as a feed back element. Therefore, it is necessary to reduce drain conductance as well as to increase transconductance.

The one way to eliminate increases in drain conductance is to lengthen the gate-drain distance in spite of the gate length shortening. However, the gate-source distance should not be lengthened because it increases source resistance and degrades high frequency noise performance.

Results of a two-dimensional device simulation are shown in Fig.1. The figure shows dependence of g_d and g_m on gate-drain distance (Lgd), where the gate-source distance keeps constant of 0.2um. The g_d increase compared with the gm when gd is less than 0.3um.

A schematic diagram of an advanced SAINT-FET is shown in Fig.2. The asymmetric n^+ layer structure is fabricated by using a self-aligned implantation technology as follows. In Fig.3, a

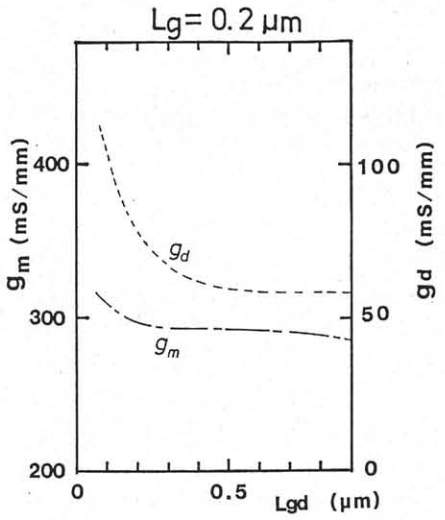

Fig.1 Dependence of g_d and g_m on the gate-source distance (Lgd) as determined by a two-dimensional device simulation.

T-shaped dummy gate was fabricated by conventional SAINT FET technology[5],[8], where Ln^+ corresponds to the distance between n^+ layers, and Lg is equal to real gate length. The real gate length is defined by the amount of "a" remaining after photoresist side-etching. Si^+ implantation for n^+ layers was performed using this T-shaped dummy gate as an implantation mask. Here, the incident beam angle was tilted 7° off the vertical on the source side. As a result, Lgd is much longer than Lgs, as shown in Fig.3. Lgd and Lgs of the fabricated device are 0.45 um and 0.25 um, respectively. Active layers were provided by selective Si^+ implantation into semi-insulating GaAs substrate at 30 KeV for the n-layer and at 200 KeV through 0.15um SiN film for the n^+-layer. The P-layer was selectively buried under the active layers by Be^+ implantation at 70 KeV.

(b) FET Characteristics

Two types of FETs, i.e., asymmetric FETs (Advanced SAINT-FETs) and symmetric FETs were fabricated.

Typical I-V characteristics of asymmetric and symmetric FETs are shown in Fig.4. Transconductance gm is 240 mS/mm (Vgs=0.4V, Vds=3.0V) in both FET structures. Drain conductance gd of asymmetric and symmetric FETs are 5.5 mS/mm and 11 mS/mm, respectively. The dependence of g_d/g_m on the gate length for a 2-inch wafer as compared with that of symmetric

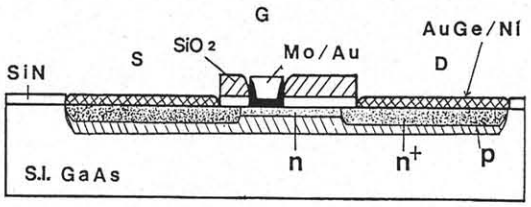

Fig.2 Schematic diagram of an asymmetric n^+ layer Advanced SAINT-FET structure.

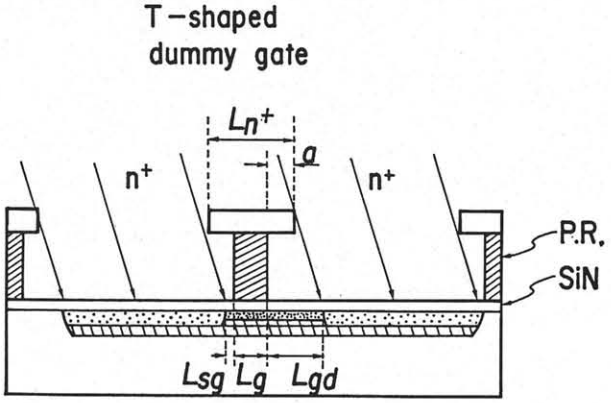

Fig.3 Self-aligned Si^+ implantation using a T-shaped dummy gate as an implantation mask. The incident beam is tilted 7° off the vertical on the source side.

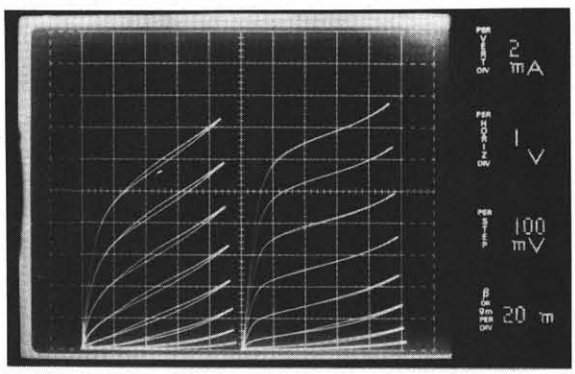

Fig.4 Typical I-V characteristics of a symmetric FET (left) and an asymmetric FET (right).

FETs is shown in Fig.5. From the figure, a 50% reduction in g_d/g_m can be observed for the asymmetric FETs. Furthermore, C_{gd} of this FET is reduced by 35% due to a large L_{gd} value (See Fig.6). The f_{max} of the FET is about 60 GHz, which represents a 20% increase due to the improvement of g_d and C_{gd}. In addition, the standard threshold-voltage deviation of the process monitor FETs with gate dimensions of 0.3 x 10 um is only 50mV over the entire area of the 2-inch wafer. This indicates a very high uniformity in spite of the short-gate FET with high f_{max}. These characteristics can occur simultaneously because the gate is defined by

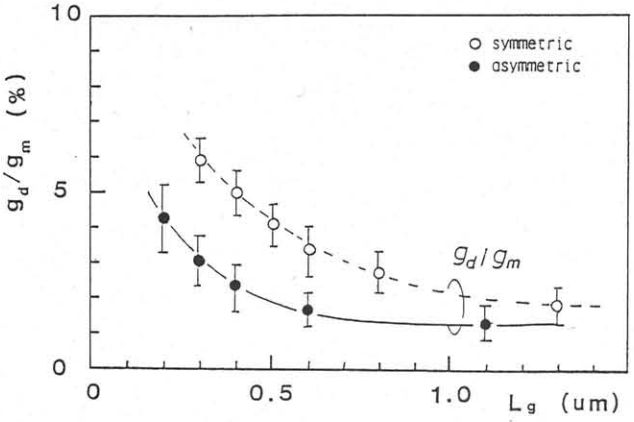

Fig.5 Dependence of g_d/g_m on gate length in a 2-inch wafer.
Symmetric FET : $L_{sg} = L_{gd} = 0.25$um
Asymmetric FET : $L_{sg} = 0.25$um, $L_{gd} = 0.45$um

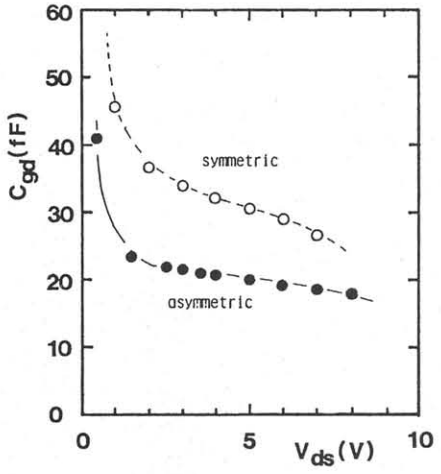

Fig.6 Reduction of C_{gd} for asymmetric FETs with gate dimensions of 0.3 x 120um.
Symmetric FET : $L_{sg} = L_{gd} = 0.25$um
Asymmetric FET : $L_{sg} = 0.25$um, $L_{gd} = 0.45$um

ordinary UV lithography by using a stepper unit and the channel under the gate is entirely unrecessed.

3. Circuit Design

A five-stage monolithic low noise amplifier (LNA) has been developed using the asymmetric n^+ layer FET. The circuit schematic for the LNA is shown in Fig.7. This LNA consists of five FETs, four resistors, sixteen MIM capacitors, microstrip transmission lines, and air-bridges. The input, output, and interstage matching networks consist of shunt shorted stubs and cascaded transmission lines. SiN MIM capacitors are employed for both RF bypassing and DC blocking applications. Shunt shorted stubs and DC blocking capacitors are also used as bias feed circuits. An optimization

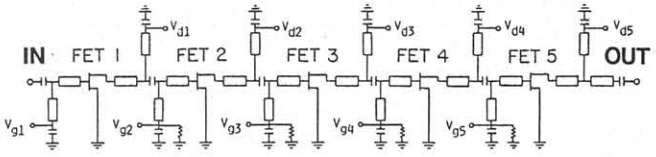

Fig.7 A circuit schematic for the five-stage LNA.

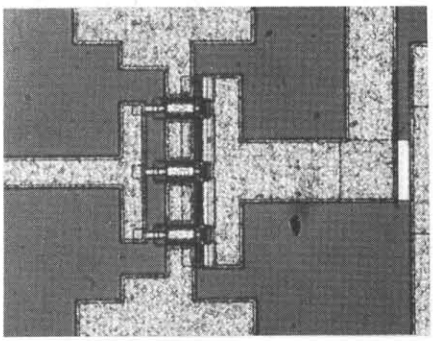

Fig.8 An Advanced SAINT-FET in LNA, where total gate width and unit gate width are 120um and 20um, respectively.

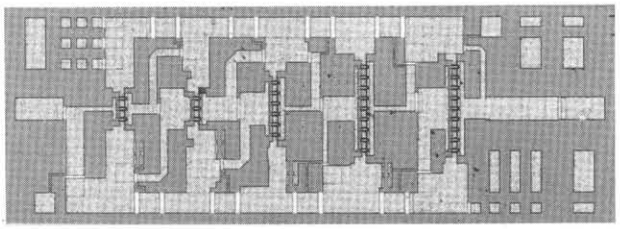

Fig.9 Microphotograph of the five-stage monolithic low noise amplifier.
Chip size is 2.8 x 0.95 x 0.15 mm.

routine was used to obtain the optimum element values to provide a noise match for the input matching network and a gain match for the interstage and output matching networks. Here, during optimization, interstage matching circuits are restricted in physical dimensions to reduce chip size. Moreover, the effects of MIM capacitors and grounded wire inductances were included in the optimization.

Advanced SAINT-FETs with gate dimensions of 0.3 x 120 um, 0.3 x 240 um, and 0.3 x 360 um, were used for an LNA. An FET with gate dimensions of 0.3 x 120 um is shown in Fig.8. The optimum unit gate width of the FET was 20 um with relation to noise performance. A completed five-stage monolithic LNA chip is shown in Fig.9. The chip size is only 2.8 x 0.95 x 0.15 mm, which corresponds to the size of an ordinary two-stage amplifier.

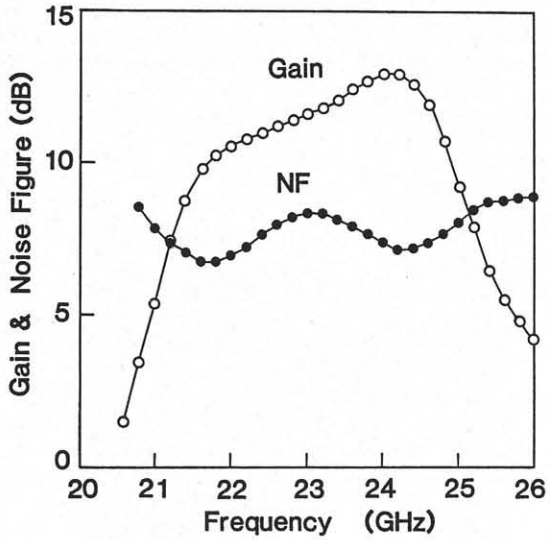

Fig.10 Measured gain and noise responses of the five-stage monolithic LNA.

4. Measured Performance

A DC-26.5 GHz band coaxial test fixture was designed and fabricated to facilitate the 20 GHz band LNA measurement. A K-connector coaxial system was employed. The return loss of a through-line test fixture was less than -15dB up to 26.5GHz.

The measured gain and noise performance of the LNA is shown in Fig.10. The LNA achieves a maximum noise figure of 8.5dB with minimum gain of 10dB, over the 21.8GHz to 24.9GHz range. The optimal noise figure was 7.0dB with a gain of 10.2dB at 21.8GHz. Furthermore, the optimal gain was 13.0dB with a noise figure of 7.5dB at 24.2GHz. Here, the LNA was left as made, and no additional tuning adjustments were made inside or outside the chip. The LNA achieves good gain and noise performances considering that uses ion implanted and self-aligned FETs, which have great advantages in uniformity and reproducibility, but which fall short in many other departments.

5. Conclusions

This is the first five-stage monolithic amplifier which operates successfully above 20 GHz. The excellent uniformity and reproducibility of an Advanced SAINT-FET makes large-scale integration possible. The information provided in this investigation contains the basis for such large-scale monolithic microwave integrated circuits (MMICs) as one-chip RF receivers above 20 GHz.

Acknowledgements

The authors wish to thank Dr.Takayuki Sugeta for his valuable advice in discussions. They are also indebted to all process members of their section for assistance in device fabrication.

References

(1) M.Feng, et al., GaAs IC Symp., pp.121-124, 1984.

(2) M.Feng, et al., Appl. Phys. Lett., pp.327-329, Nov. 1982.

(3) G.Kaelin et al., GaAs IC Symp., pp.11-12, 1983.

(4) L.C.T.Liu et al., GaAs IC Symp., pp.7-10, 1985.

(5) Y.Ishii, et al., GaAs IC Symp., pp.121-124, 1984.

(6) K.Osafune, et al., IEEE Microwave and Millimeter-wave Monolithic Circuits Symp., pp.81-85, 1986.

(7) T.Takada, et al., IEEE Trans. MTT, pp.1579-1584, Dec. 1985.

(8) T.Enoki et al., 17th Conf. on Solid State Devices and Materials, Tokyo, pp.113-118, 1985.