A High Performance LDD GaAs MESFET with a Refractory Metal Gate

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The LDD (Lightly-Doped Drain) technology was first applied to GaAs MESFETs by employing a novel combined technology involving SWAT (Sidewall-Assisted Self-Alignment Technology) and low resistivity bilayer refractory metal gate technology. The intermediate carrier concentration regions are introduced between the active layer and n+ regions, which successfully reduced the short channel effect with increasing g_m and K-values. As high as 256 mS/V-mm average K-value and 272 mS/mm average g_m value have been obtained from 0.8 µm long gate enhancement mode FETs. The minimum propagation delay of 18.5 ps/gate was obtained from a 0.8 µm gate E/D DCFL ring oscillator.

I. INTRODUCTION

In order to achieve ultrahigh-speed performance in GaAs LSIs, it is quite important to make a further improvement in the load drivability of the basic logic gates and, hence, to increase the transconductance (g_m) of GaAs MESFETs. To this end, many MESFET technologies have been developed demonstrating their potentialities, such as SAINT, refractory metal gate n+ self-alignment technology, Pt buried gate layer technology, and closely-spaced electrode technology.

Due to its essential simplicity in fabrication process, the refractory metal gate n+ self-alignment technology has been recognized to have higher potentiality for GaAs LSI technology. Thus, a variety of approaches have been made up to now to obtain a highly refined fabrication process based on the refractory metal gate technology.

This paper describes the LDD GaAs MESFET technology having a refractory metal gate, which realizes improved characteristics through a simple and stable fabrication process.

II. GaAs MESFET DESIGN

Three kinds of refractory metal gate n+ self-aligned GaAs MESFETs are compared in Fig. 1. In the conventional FET case (A), contact (n+) regions are implanted using a gate electrode as a mask. As the n+ regions are formed just adjacent to the gate, a strong short channel effect was observed unless efforts were made concerning device structure and/or processing technology improvements. The main causes for the short channel effect observed here are the lateral impurity diffusion from the n+ regions into the active layer and the substrate leakage current between the two n+ regions.

To solve this problem, the authors’ group presented structure (b) FET, where the n+ regions and the gate electrode are narrowly spaced (~0.2 µm) by using SWAT. A prototype 3k gate GaAs gate array has been developed employing this technology, demonstrating excellent performance. The only

![Fig. 1 Structures for the refractory metal gate n+ self-aligned GaAs MESFETs. Here, n' represents the intermediate carrier concentration region.](image-url)
remaining point to be improved for this technology was the parasitic source series resistance (R_s) reduction. Compared with (A), the R_s for (B) becomes larger especially for enhancement mode FETs, because the thin active layer, which is very sensitive to the surface states, stretches outside the gate electrode underneath the sidewalls.

From these viewpoints, an LDD technology was first adopted for a GaAs MESFET by employing SWAT. The new device has intermediate carrier concentration (n') regions between the n⁺ regions and the active layer under the gate, which has successfully reduced the short channel effect with increasing g_m and K-values. For realizing low resistance with small internal stress gates, a WSi_x-W bilayer refractory metal gate technology7 was combined with SWAT for the present LDD GaAs MESFET.

III. FET FABRICATION

The fabrication process for the LDD GaAs MESFET is shown in Fig. 2. First, the active (n) layer was formed by selective implantation of Si ions into LEC grown lightly Cr-doped substrates. A 0.2 μm thick WSi_x film and a 0.3 μm thick W film were successively deposited and then reactively ion-etched to form the gate electrode. After that, the wafer surface was coated by a SiO_2 film, and anisotropically dry-etched for forming sidewalls. The sidewall thickness was 0.3 μm. Using the gate and sidewalls together as a mask, Si ions were implanted for contact (n⁺) regions.

Implantation for the n' regions was performed after removing the sidewalls. Acceleration energies (E_a) and doses (Φ) for n and n⁺ regions were 30 keV, 2.5×10¹² cm⁻² and 100 keV, 3.0×10¹³ cm⁻², respectively. Three kinds of implanted layers were then activated at 800°C in H₂ atmosphere for 20 minutes. Despite the thick metal gate, the metal stress was less than 2×10⁹ dyn/cm² after post implant anneal. Ohmic electrodes were made by alloying AuGe-Ni film. A Ti-Pt-Au film was finally deposited to form the pads for each electrode.

IV. RESULTS AND DISCUSSIONS

(1) Static Characteristics Comparison

The parameters dependence on the dose for n' regions (Φ(n')) are shown in Fig. 3. The acceleration energy for n' regions was fixed at 50 keV. The parameters for FET (A) are also plotted in the figure. All the data shown are average values within a 2-inch wafer. It is clearly seen that K-value reaches its maximum at Φ(n')=7×10¹² cm⁻². The maximum value is as high as 256 mS/V-mm, which is about 40% larger, as compared with FET (A), fabricated under the same process conditions. The g_m value at 0.6 V gate bias (VGS) was 272 mS/mm for the average threshold voltage (V_T) of 0.08 V.

Gate breakdown voltage (BV_G) and the R_s value decreased monotonically as Φ(n') increased. At Φ(n')
exhibits very small voltage value. That V\textsubscript{T} value is only 31 mV, using Cr-doped substrates.

(2) Static Characteristics of the LDD GaAs MESFETs

LDD FET parameters dependence on substrate crystal orientation was investigated. In Fig. 5, parameters V\textsubscript{T0}, γ, K\textsubscript{0} and λ, which are related in the following equations, are plotted against L\textsubscript{G} for [011]- and [011]-oriented FETs.

\begin{align*}
V\textsubscript{T} &= V\textsubscript{T0} - γ V\textsubscript{DS} \quad \text{---(1)} \\
K &= K\textsubscript{0} (1+λ V\textsubscript{DS}) \quad \text{---(2)}
\end{align*}

Here, V\textsubscript{DS} denotes drain bias voltage. Although the λ value exhibited a different behavior between the two, the absolute values are sufficiently small for practical use. For example, 0.02 V\textsuperscript{-1} for λ means 4% change in K-value, when V\textsubscript{DS} increased by 2V. Except for the λ value, the FET parameter dependence on the gate orientation is very small in the full L\textsubscript{G} region.

Typical drain current-voltage characteristics for the 0.8 µm long gate enhancement mode FET are shown in Fig. 6.

(3) Dynamic Performance

Dynamic performance for the LDD FET was examined by 25 stage E/D DCFL (Direct Coupled FET Logic) ring oscillators. Gate length is 0.8 µm for enhancement (E) and depletion (D) mode FETs. Gate widths are 10 µm for E-FET and 5 µm for D-FET. The
propagation delay ($t_{pd}$) and power dissipation ($P_d$) are plotted against drain supply voltage ($V_{DD}$) in Fig. 7. At $V_{DD}=1.0$ V, $t_{pd}$ was 34.0 ps/gate with a small $P_d$, 0.96 mW/gate. The power-delay product is 3.27 fJ. The minimum $t_{pd}$ of 18.5 ps/gate was obtained with $P_d=4.5$ mW/gate at $V_{DD}=6.0$ V. The output waveform is shown in Fig. 8.

V. CONCLUSION

The LDD technology has first been applied to GaAs MESFETs, resulting in a successful reduction of the short channel effect with increasing $g_m$ and $K$-values. The average $g_m$ and $K$-values for 0.8 µm long gate E-FETs were 272 mS/mm and 256 mS/V-mm, respectively, with dynamic performance of $t_{pd}=18.5$ ps, $P_d=4.5$ mW/gate. The combined SWAT technology with low resistivity bilayer refractory metal gate technology has made fabricating high performance LDD GaAs MESFETs possible through a simple and stable processes.

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