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A High Performance LDD GaAs MESFET with a Refractory Metal Gate

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The LDD (Lightly-Doped Drain) technology was first applied to GaAs MESFETs by employing a novel combined technology involving SWAT (Sidewall-Assisted Self-Alignment Technology) and low resistivity bilayer refractory metal gate technology. The intermediate carrier concentration regions are introduced between the active layer and n+ regions, which successfully reduced the short channel effect with increasing g_m and K-values. As high as 256 mS/V·mm average K-value and 272 mS/mm average g_m value have been obtained from 0.8 μm long gate enhancement mode FETs. The minimum propagation delay of 18.5 ps/gate was obtained from a 0.8 μm gate E/D DCFL ring oscillator.

I. INTRODUCTION

In order to achieve ultrahigh-speed performance in GaAs LSIs, it is quite important to make a further improvement in the load drivability of the basic logic gates and, hence, to increase the transconductance (g_m) of GaAs MESFETs. To this end, many MESFET technologies have been developed demonstrating their potentialities, such as SAINT[1], refractory metal gate n+ self-alignment technology[2], Pt buried gate layer technology[3], and closely-spaced electrode technology[4].

Due to its essential simplicity in fabrication process, the refractory metal gate n+ self-alignment technology has been recognized to have higher potentiality for GaAs LSI technology. Thus, a variety of approaches have been made up to now to obtain a highly refined fabrication process based on the refractory metal gate technology.

This paper describes the LDD GaAs MESFET technology having a refractory metal gate, which realizes improved characteristics through a simple and stable fabrication process.

II. GaAs MESFET DESIGN

Three kinds of refractory metal gate n+ self-aligned GaAs MESFETs are compared in Fig. 1. In the conventional FET case (A), contact (n+) regions are implanted using a gate electrode as a mask. As the n+ regions are formed just adjacent to the gate, a strong short channel effect was observed [5] unless efforts were made concerning device structure and/or processing technology improvements. The main causes for the short channel effect observed here are the lateral impurity diffusion from the n+ regions into the active layer and the substrate leakage current between the two n+ regions.

To solve this problem, the authors' group presented structure (b) FET , where the n+ regions and the gate electrode are narrowly spaced (~0.2 μm) by using SWAT[4]. A prototype 3k gate GaAs gate array has been developed employing this technology, demonstrating excellent performance.[6] The only

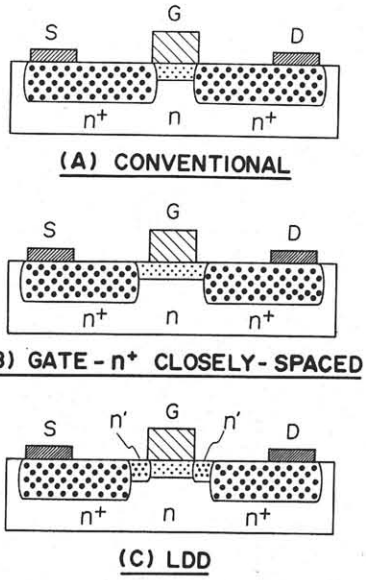

Fig. 1 Structures for the refractory metal gate n+ self-aligned GaAs MESFETs. Here, n' represents the intermediate carrier concentration region.

remaining point to be improved for this technology was the parasitic source series resistance (R_S) reduction. Compared with (A), the R_S for (B) becomes larger especially for enhancement mode FETs, because the thin active layer, which is very sensitive to the surface states, stretches outside the gate electrode underneath the sidewalls.

From these viewpoints, an LDD technology was first adopted for a GaAs MESFET by employing SWAT. The new device has intermediate carrier concentration (n') regions between the n+ regions and the active layer under the gate, which has successfully reduced the short channel effect with increasing g_m and K-values. For realizing low resistance with small internal stress gates, a WSi_x-W bilayer refractory metal gate technology[7] was combined with SWAT for the present LDD GaAs MESFET.

III. FET FABRICATION

The fabrication process for the LDD GaAs MESFET is shown in Fig. 2. First, the active (n) layer was formed by selective implantation of Si ions into LEC grown lightly Cr-doped substrates. A 0.2 μm thick WSi_x film and a 0.3 μm thick W film were successively deposited and then reactively ion-etched to form the gate electrode. After that, the wafer surface was coated by a SiO_2 film, and anisotropically dry-etched for forming sidewalls. The sidewall thickness was 0.3 μm. Using the gate and sidewalls

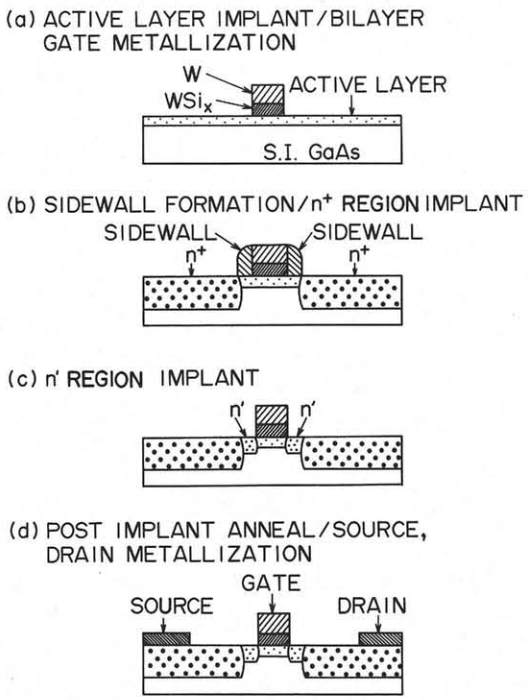

Fig. 2 LDD GaAs MESFT fabrication process.

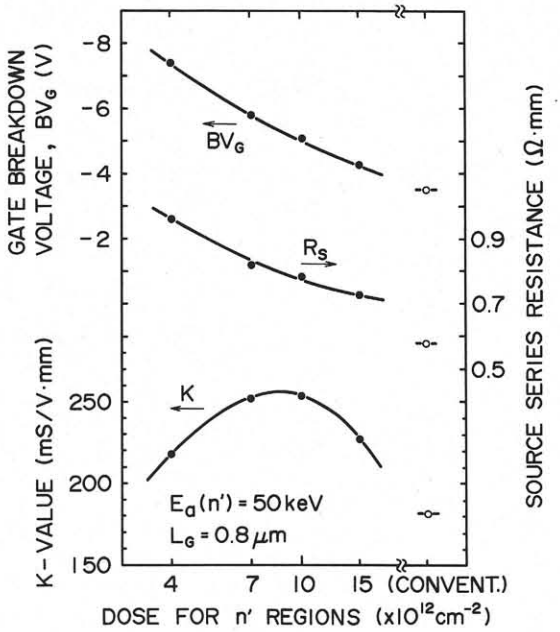

Fig. 3 LDD FET parameters dependence on dose for n' regions.

together as a mask, Si ions were implanted for contact (n+) regions.

Implantation for the n' regions was performed after removing the sidewalls. Acceleration energies (E_a) and doses (Φ) for n and n+ regions were 30 keV, 2.5×10^{12} cm^{-2} and 100 keV, 3.0×10^{13} cm^{-2}, respectively. Three kinds of implanted layers were then activated at 800°C in H_2 atmosphere for 20 minutes. Despite the thick metal gate, the metal stress was less than 2×10^9 dyn/cm^2 after post implant anneal.[7] Ohmic electrodes were made by alloying AuGe-Ni film. A Ti-Pt-Au film was finally deposited to form the pads for each electrode.

IV. RESULTS AND DISCUSSIONS

(1) Static Characteristics Comparison

The parameters dependence on the dose for n' regions (Φ(n')) are shown in Fig. 3. The acceleration energy for n' regions was fixed at 50 keV. The parameters for FET (A) are also plotted in the figure. All the data shown are average values within a 2-inch wafer. It is clearly seen that K-value reaches its maximum at $\Phi(n')=7\sim10\times10^{12}$ cm^{-2}. The maximum value is as high as 256 mS/V·mm, which is about 40% larger, as compared with FET (A), fabricated under the same process conditions. The g_m value at 0.6 V gate bias (V_{GS}) was 272 mS/mm for the average threshold voltage (V_T) of 0.08 V.

Gate breakdown voltage (BV_G) and the R_S value decreased monotonically as Φ(n') increased. At Φ(n')

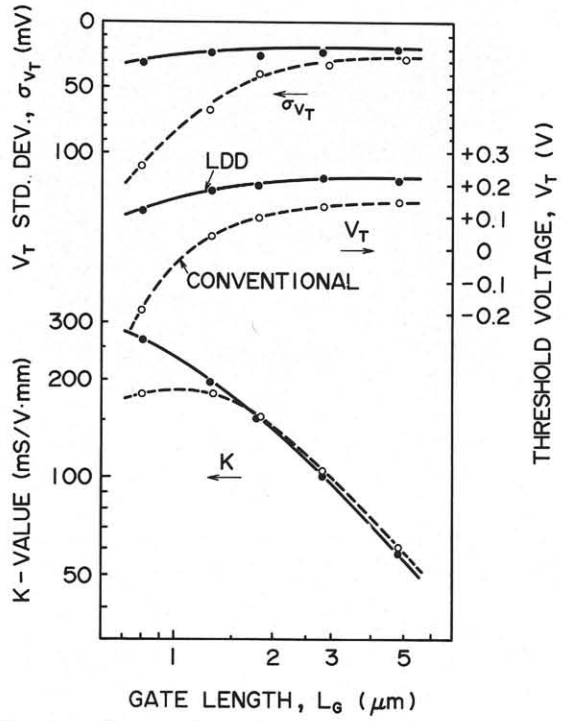

Fig. 4 Comparison between FET parameters dependence on gate length.

$=7\times10^{12}$ cm-2, the BV_G became up to -5.8 V, an about 60% improved value over that for FET (A). The R_S value at this $\Phi(n')$ was 0.82Ω·mm ($V_T=0.08$ V). The K-value degradation in the lower $\Phi(n')$ region in Fig. 3 is mainly caused by the R_S increase, due to the lower carrier concentration in the n' regions. In a higher $\Phi(n')$ region, a possible reason for decreasing K-value is the active layer thickness increase due to the lateral impurity diffusion, from the n' regions.

In Fig. 4, the FET parameters dependences on gate length (L_G) are compared between LDD and conventional GaAs MESFETs. The $\Phi(n')$ was 7×10^{12} cm-2. A marked difference is that the K-value for the LDD FETs continues to increase, as the L_G value reduces down to 0.8 μm, which in the conventional FET case, it tends to saturate in less than 2 μm long gate length region. Considering the strong V_T value shift seen in Fig. 4, the K-value saturation behavior for FET (A) is considered to be brought about by the active layer thickness increase, due to the lateral impurity diffusion from the n+ regions.

As the lateral impurity diffusion effect was greatly suppressed with the LDD technology, the short channel effect was sufficiently reduced. The threshold voltage shift was as small as -40 mV, when the L_G value varied from 4.8 μm to 0.8 μm. It is also noted that V_T standard deviation value for the LDD FET exhibits very small dependence on L_G. The maximum value is only 31 mV, using Cr-doped substrates.

(2) Static Characteristics of the LDD GaAs MESFETs

LDD FET parameters dependence on substrate crystal orientation was investigated. In Fig. 5, parameters V_{T0}, γ, K_0 and λ, which are related in the following equations, are plotted against L_G for [011]- and [01$\bar{1}$]-oriented FETs.

$$V_T = V_{T0} - \gamma V_{DS} \quad \text{-----(1)}$$

$$K = K_0 (1+\lambda V_{DS}) \quad \text{-----(2)}$$

Here, V_{DS} denotes drain bias voltage. Although the λ value exhibited a different behavior between the two, the absolute values are sufficiently small for practical use. For example, 0.02 V-1 for λ means 4% change in K-value, when V_{DS} increased by 2V. Except for the λ value, the FET parameter dependence on the gate orientation is very small in the full L_G region.

Typical drain current-voltage characteristics for the 0.8 μm long gate enhancement mode FET are shown in Fig. 6.

(3) Dynamic Performance

Dynamic performance for the LDD FET was examined by 25 stage E/D DCFL (Direct Coupled FET Logic) ring oscillators. Gate length is 0.8 μm for enhancement (E) and depletion (D) mode FETs. Gate widths are 10 μm for E-FET and 5 μm for D-FET. The

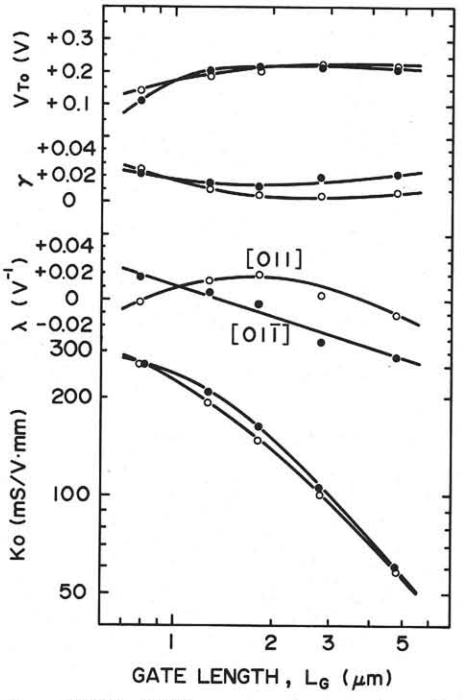

Fig. 5 LDD FET parameters gate orientation dependence. ($E_a(n')=50$keV, $\Phi(n')=7\times10^{12}$ cm-2)

propagation delay (t_{pd}) and power dissipation (P_d) are plotted against drain supply voltage (V_{DD}) in Fig. 7. At $V_{DD}=1.0$ V, t_{pd} was 34.0 ps/gate with a small P_d, 0.96 mW/gate. The power-delay product is 3.27 fJ. The minimum t_{pd} of 18.5 ps/gate was obtained with $P_d=4.5$ mW/gate at $V_{DD}=6.0$ V. The output wave form is shown in Fig. 8.

V. CONCLUSION

The LDD technology has first been applied to GaAs MESFETs, resulting in a successful reduction of the short channel effect with increasing g_m and K-values. The average g_m and K-values for 0.8 μm long gate E-FETs were 272 mS/mm and 256 mS/V·mm, respectively, with dynamic performance of $t_{pd}=18.5$ ps, $P_d=4.5$ mW/gate. The combined SWAT technology with low resistivity bilayer refractory metal gate technology has made fabricating high performance LDD GaAs MESFETs possible through a simple and stable processes.

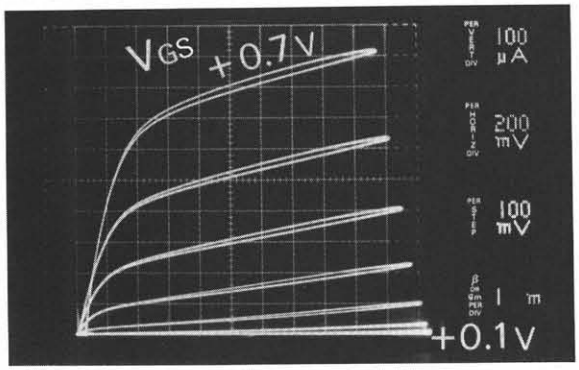

Fig. 6 Typical drain current – voltage characterisitics for LDD FET. ($L_G=0.8$ μm, $W_G=10$ μm, $V_T=0.07$ V)

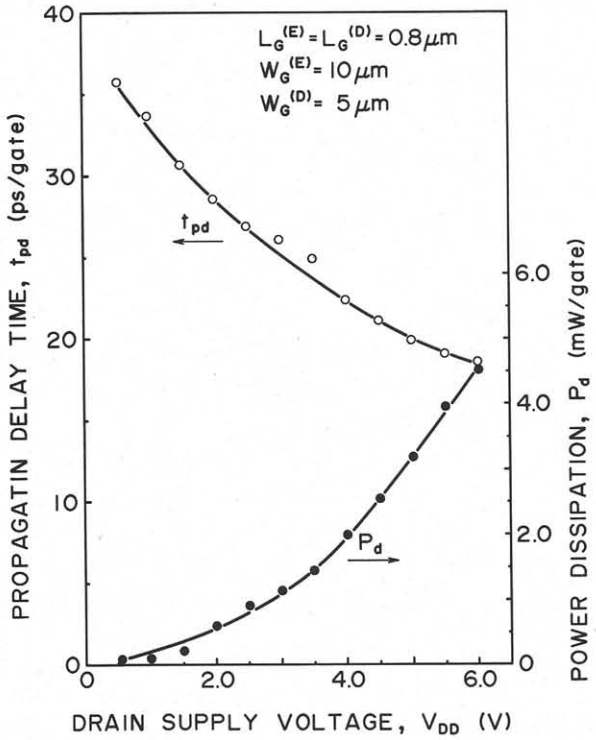

Fig. 7 Propagation delay time and power dissipation dependence on drain supply voltage.

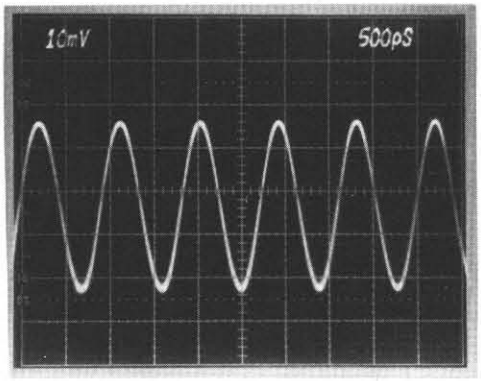

Fig. 8 Output waveguide from a 25 stage E/D DCFL ring oscillator. ($V_{DD}=6.0$ V, $t_{pd}=18.5$ ps/gate, $P_d=4.5$ mW/gate)

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