A Buried P-Layer Lightly Doped Drain (BPLDD) Self- Aligned GaAs MESFET

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A novel self-aligned GaAs MESFET (BPLDD; Buried P-layer Lightly Doped Drain Field Effect Transistor) is proposed for high speed GaAs submicron LSI's. Using this technique, short channel effect is successfully suppressed for gate length down to 0.5μm with improved K-value and transconductance. Source-to-gate breakdown voltage is also increased by this technique.

1. Introduction

Self-aligned MESFET technique using refractory metal gate has been widely used for GaAs LSI's such as 4Kb SRAM's and 16x16 bit parallel multiplier, because low source series resistance (R_s) and therefore high transconductance (g_m) are easily obtained with simple fabrication process by this technique.

However, since source/drain n^+ region is adjacent to gate metal, the conventional self-aligned MESFET has serious problems as follows.

(1) Threshold voltage (V_th) depends strongly on gate length and shifts steeply negative with shortening gate length, especially below 1μm. This is called short channel effect and causes poor controllability and uniformity of V_th.

(2) K-value decreases with shortening gate length in accordance with V_th shift. This is a serious disadvantage for high speed GaAs LSI's.

(3) Further, gate-to-source breakdown voltage (BVgs) is low.

In order to realize high speed GaAs LSI's with reasonable controllability and reproducibility, these problems should be solved. It is thought that how to minimize leakage current between source and drain, and separate source/drain n^+ region from gate metal without decreasing K-value are essential.

From these points of view, two types of self-aligned MESFET's having modified structures have been studied. One has source/drain n^+ region formed by Si ions implantation through a dielectric film (named n^+ through implantation MESFET) to separate source/drain n^+ region from gate metal. The other one is first proposed in this paper, and has source/drain n^+ region surrounded by p-layer and a lightly doped drain (named BPLDD MESFET; Buried P-layer Lightly Doped Drain MESFET).

In this paper, at first, the former is discussed in comparison with the conventional one and the problems to be solved are clarified. Based on this investigation, BPLDD MESFET is finally proposed for high speed GaAs submicron LSI's.

2. n^+ through implantation MESFET

To suppress short channel effect and obtain high BVgs, n^+ through implantation MESFET is studied. The structure is shown in Fig.1 comparing with the conventional one. Different from the conventional one, source/drain n^+
region is separated from gate metal. Fabrication process is as follows.

(1) Selective ion implantation(30KeV) and annealing(800°C) for active layer formation.
(2) WSi_x gate formation (sputtering and reactive ion etching).
(3) Dielectric film formation (p-CVD SiN; 2500Å).
(4) n^+ implantation (180-280KeV) and annealing (800°C) for source/drain n^+ region.

As same as the conventional one, source/drain n^+ region can be self-aligned. But, in this structure, it should be noted that n^+ implantation energy and/or thickness of SiN film are required to be optimized in order to suppress the short channel effect and increase BVgs without decreasing K-value. In this study, n^+ implantation energy is varied from 180 to 280KeV using a constant SiN thickness of 2500Å.

Figure 2 shows sub-threshold factor (N_g), V_th, and K-value versus gate length. BVgs is also plotted in Fig.3 against n^+ implantation energy. Improvement in both short channel effect and BVgs is observed for the n^+ implantation energy less than 200KeV. But, remarkable decrease in K-value is observed for this implantation condition. This is due to the increase in R_s as shown in Fig.4.

These results suggest that there is a trade-off between improvement of short channel effect and BVgs, and K-value. In n^+ through implantation MESFET, short channel effect and BVgs cannot be improved without decreasing K-value.

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**Fig.1** Cross-sectional view of the conventional FET(a) and n^+ through implantation FET(b).

**Fig.2** N_g, V_th and K-value versus gate length with n^+ implantation energy of 180(○), 200(△) and 240KeV(○).

**Fig.3** BVgs versus n^+ implantation energy.

**Fig.4** R_s versus n^+ implantation energy.
3. BPLDD MESFET

Figure 5 shows a cross sectional view of BPLDD MESFET. In this structure, source/drain n⁺ region is surrounded by p-layer. Gate metal is separated from source/drain n⁺ region by n' region. P-layer and n' region are expected to suppress leakage current between source and drain, and reduce R₉, respectively. Thus, improvement in both short channel effect and BVgs can be expected with higher K-value even for submicron gates.

Fabrication steps are shown in Fig.6. After active layer formation by a selective ion implantation(50KeV), WSiₓ gate are formed on an undoped semi-insulating LEC GaAs substrate by sputtering and reactive ion etching technique (a). Then, Be ions are implanted(60KeV) using WSiₓ gate as a mask (b). Source/drain n⁺ region is formed by Si ions implantation(230KeV) through a SiN film (2000Å) (c). Finally, source/drain ohmic contact (alloyed AuGe) is formed (d). Due to p-layer surrounding source/drain n⁺ region and n' region(compensated by Be ions), higher energy can be adopted for n⁺ implantation. Therefore, sheet resistance of n' is considerably reduced by lateral spread of n⁺, which gives low R₉.

Figure 7 shows gate length dependences of N₉, Vth and K-value. As shown in this figure, much improvement is achieved by BPLDD MESFET. No remarkable short channel effect is observed for the gate length down to 0.5μm. Vth is independent on gate length and K-value increases with decreasing gate length down to 0.5μm. Very small N₉ of 1.8 is obtained for 0.5μm gate.

Figure 8 shows typical I-V characteristics of BPLDD MESFET(Vth=1.25V for 0.5μm). High Transconductance of 300mA/mm is obtained for the FET with Vth=60mV.
Dovolco parameters

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<th>BVgs (V)</th>
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Table 1 Device characteristics of three types of FET's (W_g=20μm).

4. Summary

A novel self-aligned GaAs MESFET technique (BPLDD) is proposed for high speed GaAs submicron LSI's. Using this technique, excellent FET performances described below are realized.

1. No remarkable short channel effect is observed for gate length down to 0.5μm.
2. High transconductance of 300mS/mm and K-value of 6mA/V^2 are obtained for 0.5μm gate FET (W_g=20μm).
3. Source-to-gate breakdown voltage (BVgs) is also improved and BVgs of 8V is obtained.

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References

1. N.Yokoyama et al., 1984 ISSCC Digest of Technical Papers, p.44(Feb) 1984.