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Formation of MESFETs in GaAs/$Ca_xSr_{1-x}F_2$/GaAs SOI Structure

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SOI-GaAs structures of GaAs/$Ca_xSr_{1-x}F_2$/GaAs were grown by molecular beam epitaxy, and MESFETs were fabricated in the SOI layers for the first time. Electron mobilities of SOI layer were improved by use of two step growth technique and optimization of lattice matching condition. Hall mobility of $2700cm^2V^{-1}s^{-1}$ was obtained in the $4x10^{17}cm^{-3}$ Si doped SOI layer. Trans-conductance, g_m, of FET on the SOI-GaAs layer was observed to be 25mS/mm with 3μm gate length.

1. Introduction

It is very attractive to form compound semiconductor SOI (semiconductor on insulator) structure for future high-speed, multi-function and three dimensionally integrated circuits, because low dielectric constant of insulator films reduces parasitic capacitance, and different kind of semiconductors (for example GaAs and Si, etc.) can be integrated monolithically with perfect electrical isolation between the semiconductor layers.

Promising approaches to realize compound semiconductor SOI structure are heteroepitaxy of semiconductor and crystalline insulator. Mixed crystal of group-IIa fluorides, $Ca_xSr_{1-x}F_2$, have many advantage for insulator material such as 1) facility of low temperature epitaxial growth on semiconductors (<500°C), 2) widely variable lattice constant (5.46-5.80A) which makes possible lattice matching to various kinds of semiconductors, and 3) low dielectric constant (6.5-6.8)[1-3].

Formation of GaAs/$Ca_xSr_{1-x}F_2$/GaAs[4-6] and GaAs/CaF_2/Si[7] has been reported. In these works, Siskos et al. reported mobilities of electrons in SOI-GaAs layer, however, optimization of growth condition from viewpoints of electrical characteristics has not been discussed yet.

GaAs/Insulator/Si(Substrate) structure is more attractive for device applications rather than GaAs/Insulator/GaAs(Substrate) structure as being indicated by recent activity of researches for GaAs/Si structure[8-10]. In this work, however, GaAs/$Ca_xSr_{1-x}F_2$/GaAs structure was used because it is free from problems of difference of lattice constant and thermal expansion coefficient between the SOI film and substrate. Two step growth technique and lattice matching condition which depends on temperature were investigated to obtain SOI-GaAs with good electrical properties and, for the first time, MESFETs were fabricated in the SOI-GaAs structure. These results are considered to be applicable to SOI-GaAs structure of GaAs/Fluoride/Si.

2. Growth of GaAs-SOI structures

GaAs/$Ca_xSr_{1-x}F_2$/GaAs structures were grown by two way processes as shown in Fig.1 using molecular beam epitaxy. In process A[4], growth of $Ca_xSr_{1-x}F_2$ on GaAs substrates and growth of SOI-GaAs layers on them were carried out with two separate systems. 120-150nm-thick $Ca_xSr_{1-x}F_2$ films were grown by vacuum evaporation onto the thermal-cleaned(580°C,5min) GaAs(100) wafers at a growth temperature of 450°C. After that, SOI-GaAs films were grown in another MBE

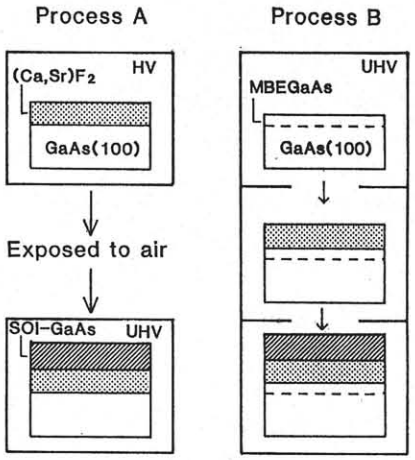

Fig.1 Growth process of SOI structure. Process A is a separated growth and process B is a in-situ growth using two growth chamber system.

chamber. On the other hand, in process B, SOI structures were grown in situ without exposed to the atmosphere using the two growth chamber system, where substrates could be transferred from one chamber to the other in UHV. After 0.5μm homoepitaxial GaAs layers were grown on GaAs wafers in conventional manner, they were transferred into the fluoride growth chamber where 120nm-thick $Ca_xSr_{1-x}F_2$ films were grown at 450°C, and finally they were transferred into GaAs-MBE chamber again to grow SOI-GaAs films. In this work, mainly, investigation of growth characteristics were carried out by the process A, and growth for fabrication of MESFETs were carried out by the process B which has advantage of avoiding contamination and of realizing better surface of GaAs on which $Ca_xSr_{1-x}F_2$ were grown.

SOI-GaAs films were grown by the two-step growth technique[4], whose effects are shown in Fig.2 comparing with conventional single temperature growth by Rutherford backscattering spectroscopy (RBS) and measurements of Hall mobilities of electrons in the Si-doped SOI layers. The crystalline quality of SOI-GaAs was characterized by the normalized channeling minimum yield, χ_{min}, near the surface region. In the single temperature growth, the best value of χ_{min} was obtained at 450°C, however, this temperature is considered to be too low to realize good electrical characteristics compared to the conventional MBE growth conditions in GaAs homoepitaxy. On the other hand, in the two

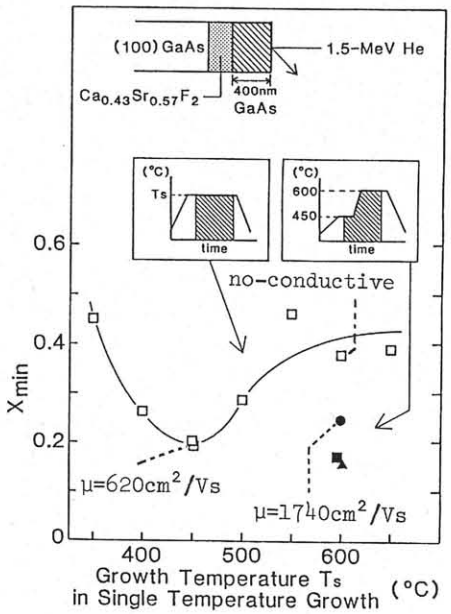

Fig.2 Effects of two step growth of SOI-GaAs layers characterized by channeling minimum yield on RBS measurements and Hall mobility of electrons.

step growth in which the growth started at 400-450°C and then the temperature was raised to 580-600°C without interrupting the growth, the χ_{min} is still low in the surface region grown at the high temperature. Electron mobilities (doping condition is the same as Fig.3(a)) in SOI-GaAs films grown by the single temperature method were poor at both temperatures of 450 and 600°C, whereas those by the two step growth were fairly improved.

According to the Vegard's law, the mixing ratio of the fluoride whose lattice constant matches to GaAs is $Ca_{0.43}Sr_{0.57}F_2$ at room temperature(R.T.). But since the thermal expansion coefficient of the fluoride is much larger than that of GaAs, the mixing ratio to satisfy the matching condition is shifted at elevated temperatures[11]. Such a lattice matching condition between GaAs and $Ca_xSr_{1-x}F_2$ was examined by evaluating electron mobilities in the SOI layers. Samples for measurements were grown by the process A whose structure is shown in Fig.3(a). $Ca_xSr_{1-x}F_2$ films were grown on GaAs(100) substrate varying mixing ratio x from 0 to 0.72. SOI-GaAs was grown by the two step growth, in which 150nm thick undoped layer was grown at 450°C, then 0.5 or 1.5μm thick undoped buffer layer and 0.5μm thick Si-doped layer($4x10^{17}cm^{-3}$) were successively grown at 580°C. Measured Hall

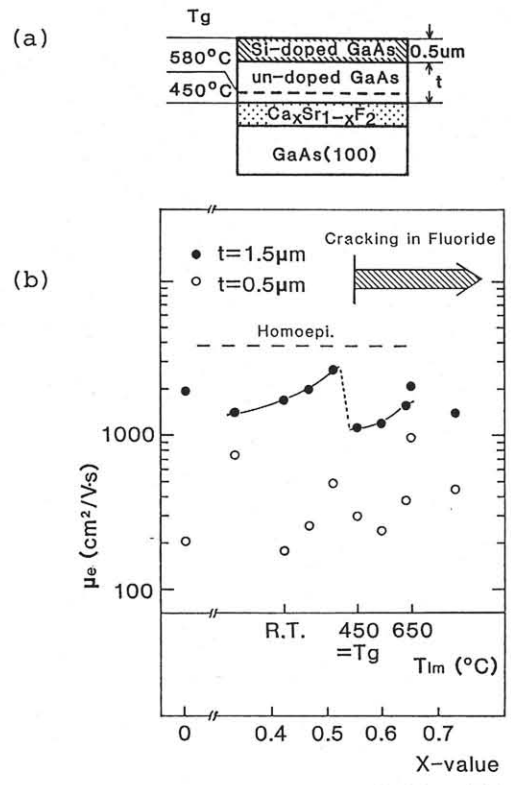

Fig.3 Relation between electron Hall mobility in SOI-GaAs and mixing ratio of fluoride. (a) shows sample structure and (b) shows results of measurements.

mobilities of electrons in the n-layer are shown in Fig.3(b) as a function of the mixing ratio of the fluorides. T_{lm} on horizontal axis means the temperature at which the $Ca_xSr_{1-x}F_2$ of corresponding x-value matches to that of GaAs. Although mobilities in the layer on thicker buffer layer show higher value, as far as in the same thickness of buffer layer, it can be seen that mobilities increase as the x-value increases from x=0.43 to x=0.56, i.e., from T_{lm}=R.T. to T_{lm}=450°C, the latter corresponds growth temperature of $Ca_xSr_{1-x}F_2$ and that of SOI-GaAs at start of two step growth. In the region of x>0.56, however, it can be seen that mobilities decrease discontinuously. It has been found that the decrease is due to crack generation in the fluoride film before growth of SOI-GaAs.

These experimental results show that higher electron mobilities are obtained when the mixing ratio of fluoride is so chosen that lattice matching condition is satisfied at near growth temperature rather than R.T. The highest mobility observed in SOI-GaAs was 2700$cm^2V^{-1}s^{-1}$ which was about 70% of that obtained in homo-epitaxial GaAs layers grown at the same time.

3. Fabrication of MESFETs in SOI-GaAs layers

SOI structures for fabrication of MESFETs were grown by the process B as described above. The structure of SOI substrates is shown in Fig.4(a). Mixing ratios of $Ca_xSr_{1-x}F_2$ were chosen as x=0.50-0.55 considering the experimental results shown in Fig.3. No trace of cracking in the $Ca_xSr_{1-x}F_2$ film was observed on the surface morphorogy of SOI-GaAs films. In the two step growth of SOI-GaAs, low temperature growth layers 75-150nm thick were grown at 400-450°C followed by growth at 580°C. 0.20-0.25μm of active layers doped by Si(2-3x$10^{17}cm^{-3}$) were grown on the 1.5μm-thick un-doped buffer layers.

On the surface of the SOI structure substrates, Schottky gate MESFETs were fabricated in a conventional manner. First, each device was isolated by mesaetching of active layer in $5H_2SO_4$:H_2O_2:H_2O solution. Sources and drains were formed by Au/Au-Ge using lift-off technique followed by sintering at 450°C for 90s in N_2 atmosphere, and finally Au gate electrodes were formed also by lift-off technique, as shown in Fig.4(b).

Fig.5 is an optical micrograph of a fabricated SOI-GaAs MESFET. Gate length (Lg) and gate width (Wg) are 3.0μm and 60μm, respectively. Though, the surface morphorogy of SOI-GaAs was not so good in the present state, there was no problem in fabrication of devices of such a dimension.

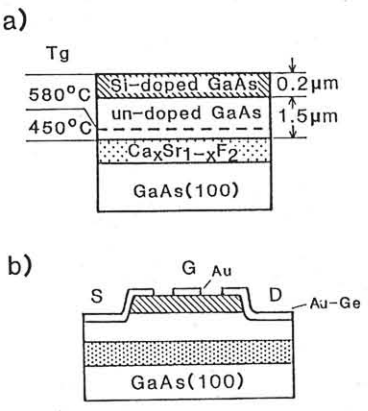

Fig.4 (a) SOI structure for fabrication of MESFETs. (b) MESFET fabricated on the substrate shown in (a).

Figure 6 shows a typical I_d-V_d characteristics of MESFET on the SOI layer. Normal FET operation was observed and g_m=25mS/mm was obtained at V_g=0.0V (L_g=3.0μm and V_t=-3.3V). The device characteristics in Fig.6 are shown in Table 1 as 'SOI-1'. Comparing the reference device fabricated on homoepitaxial substrate, g_m and K-value are rather low. This degradation must be due to low electron mobility of SOI active layer, and this means that the results shown in Fig.3(b) were not reproduce on the 'SOI-1' substrate. Indeed, the sampl 'SOI-2' shown in Table 1 showed higher K-value, though it was grown by the process A and it has large lattice mismatch(x=0.72). So, better device characteristics will be realized by optimizing the growth conditions.

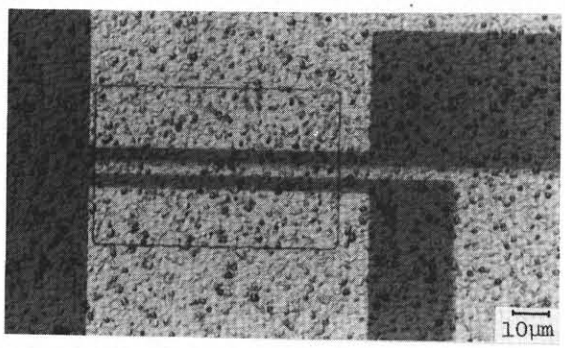

Fig.5 Optical micrograph of a MESFET with L_g=3.0μm on an SOI substrate.

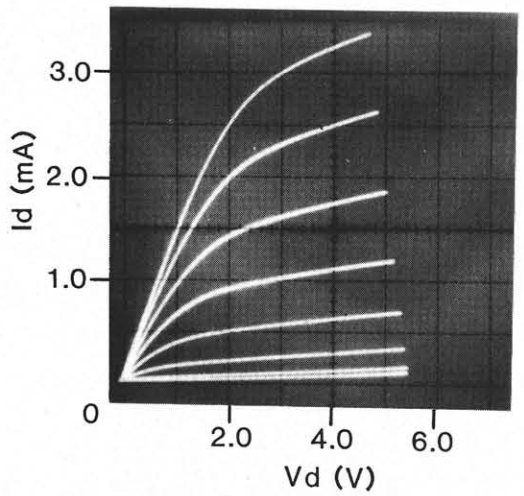

Fig.6 I_d-V_d characteristics of a MESFET on SOI-GaAs layer. V_g : from 0.0V to -3.5V in -0.5V step.

Table-1 Comparison of FET characteristics on SOI-GaAs layers and homoepitaxial GaAs substrate for a reference.

Sample	L_g(μm)	W_g(μm)	g_m(mS/mm)	K (mA/V^2)
Homoepitaxy	3.0	60	70	1.7
SOI-1	3.0	60	25	0.27
SOI-2	10.0	140	9.0	0.80

4. Conclusion

GaAs/$Ca_xSr_{1-x}F_2$/GaAs structures with good electrical properties in SOI layers were obtained by the two step growth technique and optimizing lattice matching condition.

MESFETs were fabricated in these SOI-GaAs films for the first time, and the observed g_m value was 25mS/mm for L_g=3.0μm. Though these results are still primitive, they show that such SOI-GaAs structure as GaAs/$Ca_xSr_{1-x}F_2$/GaAs and maybe GaAs/$Ca_xSr_{1-x}F_2$/Si (with gradual change of x-value in fluoride) has feasibility for device applications.

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References

1) H.Ishiwara and T.Asano; Proc. of the 14th Conf. on Solid State Device, Tokyo 1982, JJAP, Suppl22-1, p.201 (1983)
2) J.M.Phillips and J.M.Gibson; Proc. of Material Research Society vol.25 p.381 (1985)
3) K.Tsutsui, H.Ishiwara, T.Asano and S.Furukawa; Appl. Phys. Lett. vol.46 p.1131 (1985)
4) K.Tsutsui, H.C.Lee, H.Ishiwara, T.Asano and S.Furukawa; GaAs and Related Compounds 1985, Inst. Phys. Ser. No.79, Adam Hilger Ltd. p.109 (1986)
5) S.Siskos, C.Fontaine and A.M-Yague; Appl. Phys. Lett. vol.44 p.1146 (1984)
6)P.W.Sullivan, G.M.Metze and J.E.Bower; J. Vac. Sci. Technol. vol.B3 p.500 (1985)
7) T.Asano, H.Ishiwara, H.C.Lee, K.Tsutsui and S.Furukawa; Ext. Abs. of the 17th Conf. on Solid State Device and Materials Tokyo 1985 p.217 (1985)
8) R.Fischer, T.Henderson, J.Klem, W.T.Masselink, W.Kopp, H.Morkoc and C.W.Litton; Electro. Lett. vol.22 p.945 (1984)
9) M.Akiyama, Y.Kawarada, and K.Kaminishi; JJAP vol.23 L843 (1984)
10) R.Fischer D.Neuman H.Zabel H.Morkoc C.Choi and N.Otsuka; Appl Phys. Lett. vol.48 p.1223 (1986)
11) K.Tsutsui, H.Ishiwara and S.Furukawa; Appl Phys. Lett. vol.48 P.587 (1986)