Improved Reliability in Amorphous Silicon Thin Film Transistors

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The threshold voltage shift of a-Si TFT's for various fabrication conditions is discussed. The fabrication conditions have been optimized to obtain an improved a-Si /SiN interface and deposition temperature is chosen between 300°C and 360°C in contrast to a conventional range of 200-300°C. Estimation of the threshold voltage shift of our optimized samples is as low as -0.7V for a negative voltage stress of 20V for a supposed lifespan of 10^4 hours operation. This is quite acceptable for an LCD panel.

1. Introduction

Recently, there has been considerable amount of study on amorphous silicon thin film transistors(a-Si TFT's) for application to active matrix liquid crystal display panels, whose features are feasibility of full-colored display, low power consumption, lightweight, etc. Some of the advantages of a-Si TFT's are good switching characteristics, capability of large area deposition, reproducibility, and a low temperature fabrication process. Our a-Si TFT's achieve a high ratio of Ion/Ioff exceeding 7 orders of magnitude with a subthreshold slope as steep as 0.3V/decade. It has been shown that these values are sufficient for a switching matrix application[1].

However, the instability of a-Si TFT's, i.e., the threshold voltage(Vt) shift during their operation, still poses a serious problem. This instability has been investigated in various stress voltage conditions. Above all, it has been found that the Vt shift is mainly caused by applying the gate voltage. The amount of Vt shift (ΔVt) as a function of time and temperature in addition to the gate bias has also been studied. These dependences have been formulated and used to estimate the ΔVt after a certain operating time, e.g., 10^4 hours[2].

It has been suggested[3] that the quality of interface between a-Si and silicon nitride(SiN) or the density of charge trap levels at/near the interface plays an important role in the Vt shift. We have found that the fabrication condition of a-Si TFT's is closely related to the interface quality.

In this paper, we report the optimization of fabrication conditions to reduce the ΔVt by improving the interface quality between a gate insulator of SiN and a-Si. Also, the estimate of the threshold voltage shift of such optimized a-Si TFT's is presented.

2. Experiment

The cross-sectional view of a-Si TFT's is shown in Fig.1. The configuration of TFT's has a bottom gate staggered structure with a gate insulator of SiN. On the glass substrates, both SiN and a-Si film are deposited in an rf glow discharge of a gas mixture of SiH_4-NH_3-N_2 and that of SiH_4-H_2, respectively. Deposition is carried out at a substrate temperature between 200°C and 420°C.

The threshold voltage is defined as the gate voltage at the intersection of extrapolation of the saturation region in the $\sqrt{Id}$ vs. Vg curve as well as the voltage at which drain current corresponds to some value, e.g., 30nA. The amount of Vt shift is measured as the difference of Vt in before and after applying the stress voltage to
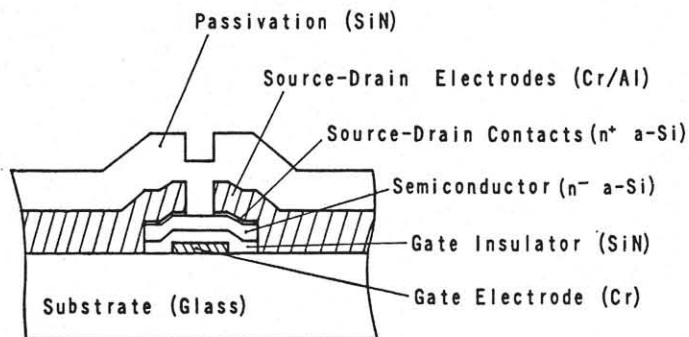
FIG. 1. Cross-sectional view of a-Si TFT.

the TFT's. The stress gate voltage is between -30V and 30V. The drain voltage has little relation to the Vt shift and is set to 0V. Before each measurement of the ΔVt, threshold voltage of a-Si TFT's is initialized by thermal annealing at 180°C for 30 minutes. This initialization procedure can be applied to the same sample more than ten times without deteriorating the device characteristics. Since amorphous silicon has high photoconductivity, all the measurements are carried out in the dark where the influence of photo-induced carriers are negligible [4].

3. Results

3.1 Vt Shift of a-Si TFT's

Figure 2 shows the Id vs. Vg characteristics of a-Si TFT's before and after dc gate bias stress of -10V and 20V for 400 hours. When a positive (negative) gate bias is applied to the TFT's, the
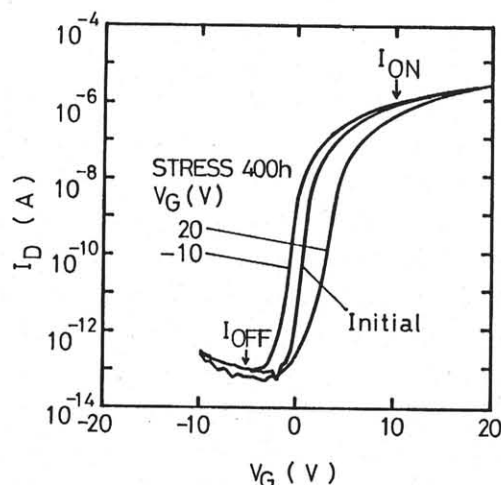

FIG. 2. Id vs. Vg characteristics before and after dc gate bias stress of -10V and 20V.

Vt is positive(negative), which implies that the Vt shift of a-Si TFT's is mainly due to the charge trapping into a gate insulator of SiN[5]. The threshold voltage shift as a function of various stress conditions has been investigated, and as for the dc bias stress, the results can be summarized in the following formula,

$$\Delta Vt \sim \alpha \cdot Vg^{\beta} \cdot (\log(t))^{\gamma} \cdot \exp(-\Delta E/kT), \qquad (1)$$

where Vg is the stress gate bias, t the operation time of a-Si TFT's, T the absolute temperature, k the Boltzmann's constant, ΔE the activation energy for charge trapping process and α, β, and γ the constants.

In the stress conditions between room temperature and 100°C, the value of ΔE has been 0.3eV for both positive and negative gate bias. The constant α depends on the fabrication conditions. The value β has been found to be 1.7 for $Vg > 0$ and is 4 for $Vg \leq 0$. It has been confirmed that γ is equal to 2 for both signs of gate voltage up to 2,000 hours. The values of these constants besides α did not scatter from run to run.

Constant α has different values for positive gate bias stress and negative bias stress. It is desirable to lower α for a negative bias, since the voltage shift under a negative bias plays a greater role than that under a positive bias which is a pulsed stress[2]. The lowered α value to realize improved reliability in TFT's is obtained as described later.

3.2 Optimization of Fabrication Conditions

High quality of the a-Si/SiN interface is necessary to improve the reliability in a-Si TFT's. To achieve this, the optimization of fabrication condition has been proved to be effective. Particularly, two ways of optimization were developed. First, the volume ratios of N_2 and NH_3 to SiH_4 in depositing chamber has been found to have a great influence on the Vt shift under stress. As the volume ratio NH_3/SiH_4 or N_2/SiH_4 is increased, the ΔVt decreased sharply and the variation of the ΔVt becomes small gradually. This is interpreted as to what extent stoichiometry in SiN is achieved,
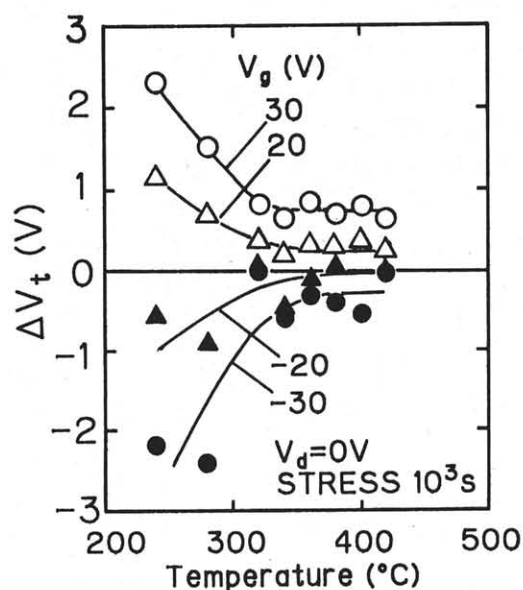
FIG. 3. Dependence of Vt shift on a-Si deposition temperature for 1,000 sec TFT operation.

FIG. 4. Dependence of on current(Vg=10V) and off current(Vg=-5V) on a-Si deposition temperature.

which means the densities of trap levels are caused by the dangling bonds of Si atoms in the silicon-rich SiN film. Consequently, from the point of view of reliability, the volume ratios of material gases are important factors.

Secondly, a more important factor to attain high reliability is the deposition temperature. In contrast to a supposed optimum a-Si deposition temperature around 200-230℃, it has been found that a temperature range higher than 300℃ is a good choice as far as reliability is concerned. Figure 3 shows the Vt shift after 1,000 sec TFT operation as a function of a-Si deposition temperature. Reduction of the voltage shift is apparent in a range higher than 300℃ for both signs of gate bias voltage. Figure 4 shows the dependence of drain current on deposition temperature. The on current(Vg=10V) decreases and the off current (Vg=-5V) increases as the temperature rises above 360℃. Below this temperature, a sufficient ratio of Ion/Ioff can be obtained indicating an optimum temperature range between 300℃ and 360℃. This temperature effect is speculated to be due to the reduction of the trap density at the a-Si/SiN interface by thermal annealing.

By the optimization described above, the α value for the negative gate bias is lowered to
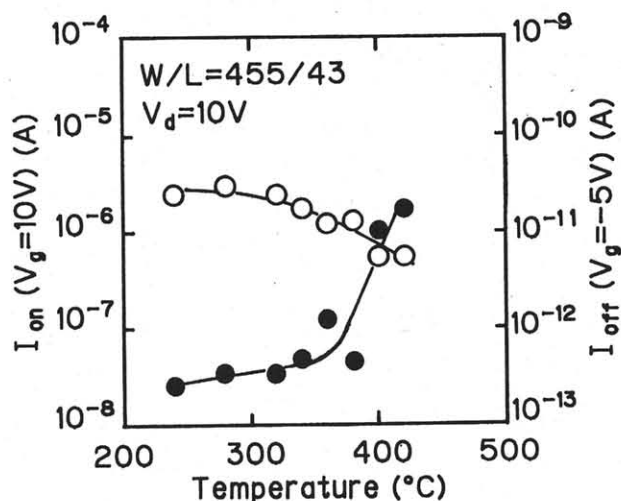
less than one fifth the previous one[2], that is, 7.5×10^{3}. The Vt shift for long term operation with a negative dc voltage of 20V can be estimated from the ΔVt for 1,000 sec by Eq. 1. For the samples fabricated at a deposition temperature of 320℃, the calculated shift is as low as -0.7V after 10^4 hours operation.

The threshold voltage shift of TFT's on the LCD panel can be estimated as follows. For the LCD panel with N gate scanning lines, TFT's are under positive bias for 1/N of operation time and under negative bias for almost the entire time. In the case N=1,000, a gate pulse height of 20V, a signal pulse of 20V from peak to peak, and 10^4 hours operation time, which are considered as reasonable values for normal use of an LCD, TFT's are under a positive bias of 20V for 10 hours and a negative bias of 20V for almost the entire time in 10^4 hours operation. The estimate of total threshold voltage shift can be obtained as the sum of the ΔVt for negative and positive bias. For our optimised a-Si TFT's fabricated at a deposition temperature of 300-360℃, the sum is less than 1V as shown in Fig. 5. For the LCD which can display gray scale, the total ΔVt is estimated to be between the above sum and the ΔVt for the positive bias(the shaded region in Fig. 5), which is also less than 1V.
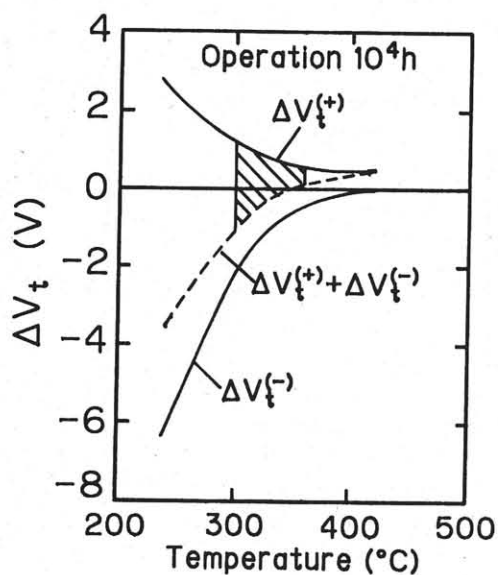
FIG. 5. Estimation of Vt shift after 10^4 hours operation vs. a-Si deposition temperature.

4. Conclusions

The threshold voltage shift of a-Si TFT's for various fabrication conditions has been optimized to improve the quality of the a-Si/SiN interface. The optimum deposition temperature range is between 300°C and 360°C. The Vt shift of our optimized sample has been estimated to be less than 1V after a supposed lifespan of 10^4 hours, which is quite an acceptable value for LCD panels.

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