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A Novel 4-Mask InSb Infrared Staring Imaging Array

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A monolithic 128 x 128 Insb array is described for staring infrared imaging systems operating in the 3 – 5μm spectral region. The array is fabricated with only 4 mask levels and has almost 4 times higher output signal and nearly 10 times greater wafer yield as compared to a previous design. The higher dynamic range has resulted in demonstration of significantly improved thermal imagery.

1. INTRODUCTION

Infrared imaging systems operating in the 3 – 5μm and 8 – 12μm spectral regions are required for many electro–optical systems in order to provide coverage for day/night and/or bad weather operation. In recent years, considerable effort has been devoted to the development of InSb and HgCdTe infrared imaging devices. For the 3 – 5μm spectral region, InSb Charge Injection Devices (CID) offer significant potential for the realization of cost–effective infrared staring imaging systems because of the relative simplicity in structure, fabrication and operation of CID arrays.[2,3] This paper describes monolithic staring imaging devices based on a novel 4–mask InSb array design. We have previously presented performance data and thermal imagery obtained from a 128 x 128 staring focal plane array. In the present work, a critical masking step has been eliminated from the process. In addition, improvements in cell design have resulted in a factor of four increase in detector array output signal. The reduction of mask levels to only 4 and the increase in dynamic range make possible the realization of large, high-yield and high-performance, monolithic infrared staring imaging arrays, such as 128 x 128. The 128 x 128 array uses a 30 x 30μm^2 unit cell size and 6.1 x 6.1 mm^2 chip size. The array design, process, and performance characteristics are described in this paper.

2. ARRAY DESIGN AND PROCESS

A new detector array design has been developed in order to improve array performance and increase fabrication yield. The performance–related improvements are discussed later. The higher fabrication yield has been realized in three ways:

1. by designing a new 30 x 30μm^2 cell with significantly relaxed design rules;
2. by eliminating one critical masking level from the process – i.e., four mask levels instead of five, and;
3. by reducing the 128 x 128 array chip size to 6.1 x 6.1 mm^2, as compared to 8.1 x 8.1 mm^2 previously. This has increased the number of chips per wafer to 16, versus 9 previously.

Figure 1 shows a photomicrograph of the new 128 x 128 InSb array. The minimum linewidth is 5μm. The chip includes 128 columns and 128 rows . Each column or row is provided with a bonding pad for interfacing to silicon chips on the focal plane substrate.

The InSb array fabrication is based on a low–temperature photon-assisted CVD process for deposition of silicon dioxide on InSb wafers. After deposition of the field oxide, the first masking step defines the active area. This is followed by deposition of the first gate oxide. Subsequently, the first layer metal is deposited and patterned to form the column electrodes *(Level 2)*.

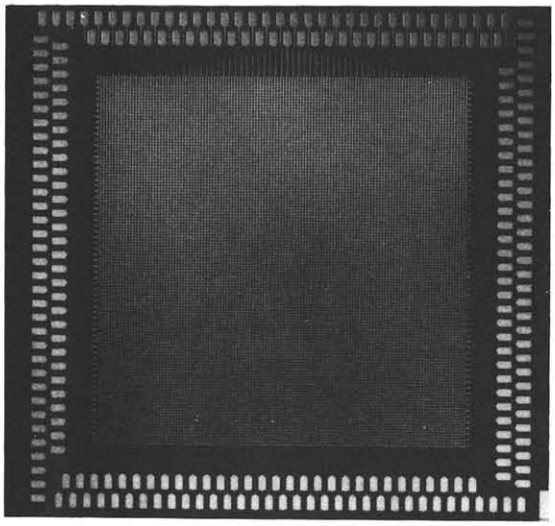

Figure 1: 128 x128 InSb Detector Array.

Next, the second gate oxide is deposited, followed by contact hole definition (*Level 3*). Finally, the second level metal is deposited and patterned (*Level 4*). The second level metal defines the rows, and also provides interconnect lines from the columns to the bonding pads. This defines a two–dimensional, monolithic staring array operating in the front–illuminated mode. No semi–transparent metal is used for an optical window. Therefore, the problems of poor transmission and non–uniformity of the semi-transparent optical window are eliminated. This has resulted in increased yield and performance.

The process outlined above is indeed simple compared to other IR detector or silicon IC fabrication processes. Only three oxide deposition and two metalization steps are required, with no need for ion implantation, diffusion, and field plates. Therefore, the process promises a high-yield, and thus a low–cost, infrared detector array technology. Based on a chip active area of 3.84 x 3.84 mm^2 and a defect density of 3/cm^2 per masking step, the anticipated wafer yield is 23% for a 4–mask process. We have exceeded this yield in actual wafer fabrication. However, with 16 chips per wafer (as compared to 9, previously), the wafer yield has increased by nearly 10X, as compared to our previous design.

3. DESIGN ANALYSIS AND EVALUATION

The performance of an imaging device is generally dependent on the dynamic range available from the device. In our approach, the InSb sensor array is integrated with silicon analog/digital LSI devices on the focal plane substrate. Digital CMOS ICs are used to drive the rows, and analog CMOS ICs are used to measure the analog photo–signals on the columns. In this approach, the photo–signal generated by a pixel on each column of the array is amplified by a silicon preamplifier. Assuming electronics noise from external circuitry can be neglected, the dynamic range is approximately given by:

$$S_{max} = \frac{qN_{max}}{C_o V_n} \tag{1}$$

where q is the electron charge, N_{max} is the charge capacity per cell of the InSb array, C_o is the output capacitance per column of the array, and V_n is the total RMS noise voltage at the preamplifier input.

The charge capacity is a function of the maximum deep–depletion electric field in InSb, the donor concentration, the oxide thickness, and the interface trap density. The RMS noise voltage V_n has contributions from the detector, V_{nd}, and from the preamplifier, V_{npa}:

$$V_n = (V_{nd}^2 + V_{npa}^2)^{1/2} \tag{2}$$

The detector noise has contributions from the incident background photons, interface traps (1/f noise), and thermally–generated dark current. In our devices, the storage time is sufficiently long that dark current noise can be neglected. The 1/f component is also negligible because correlated double sampling is used with a very short time period between samples. The maximum number of background noise carriers is equal to the square root of charge capacity N_{max}. The detector RMS noise voltage is then given by:

$$V_{nd} = q\sqrt{N_{max}}/C_o \tag{3}$$

From Eq. 1, it is desirable to reduce the column capacitance in order to increase the dynamic range. For two–dimensional arrays, the row–column overlap capacitance can be a significant part of the capacitance per cell. Figure 2 shows a plot of the output dynamic range versus the InSb substrate donor concentration, N_d, for a preamplifier input–referred noise voltage of 10μV. The lower curve corresponds to our previous design (CID3), with a row–column overlap capacitance, $C_{R/C}$, of 0.105 pF per cell. The top curve is for our new design (CID5) with a significantly reduced $C_{R/C}$ of 0.034 pF per cell.

Figure 3 shows the variation of dynamic range with preamplifier input-referred noise voltage, V_{npa}, with $C_{R/C}$ as a parameter. At low values of V_{npa}, both designs in Figure 3 have nearly the same dynamic range, as expected for background–limited operation (BLIP). The new design with $C_{R/C}$ = 0.034 pF has a 10% larger active area (for the same 30 x 30μm^2 unit cell) — resulting in slightly higher N_{max} and thus dynamic range at BLIP as compared to the design with $C_{R/C}$ = 0.105 pF.

The dynamic range in Figure 3 for the new design, with $C_{R/C}$ = 0.034 pF, is fairly insensitive to variations in preamplifier input–referred noise voltage. This suggests that background–limited operation is indeed achievable with 128 x 128 InSb arrays, an important feature that has previously been obtained with only linear or small two–dimensional infrared arrays in the 3–5μm spectral band.

In order to explore the effect of array size on device performance, the calculated results shown in Figure 4 are presented. These calculations are performed for N_d = 1 x $10^{14}/cm^3$ and for a maximum deep–depletion electric field of 0.7 x 10^4 V/cm, with $C_{R/C}$ and V_{npa} as parameters. Case No. 1 in Figure 4 corresponds to CID3 with $C_{R/C}$ = 0.105 pF and V_{npa} = 10μV. For Case 2, $C_{R/C}$ = 0.034 pF and V_{npa} = 10μV. Finally, Case 3 in Figure 4 corresponds to reductions in both $C_{R/C}$ and V_{npa}. In this case, BLIP can be achieved for even a 256 x 256 device. Thus, a 256 x 256 array in the new design would achieve a two–fold increase in spatial resolution while improving thermal resolution by a factor of two as compared to the 128 x 128 CID3 array.

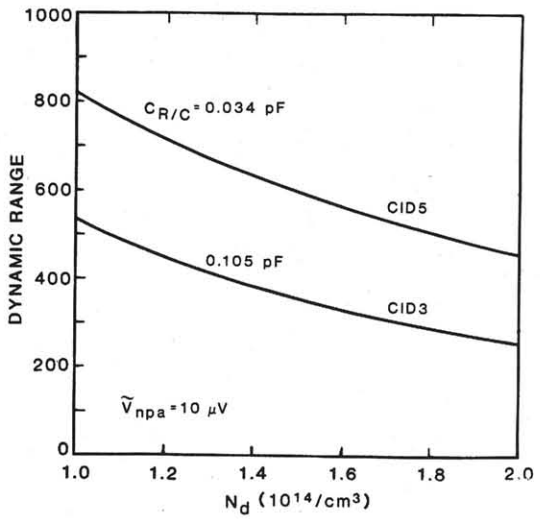

Figure 2: Plot of Output Dynamic Range vs Donor Concentration for 128 x 128 Array.

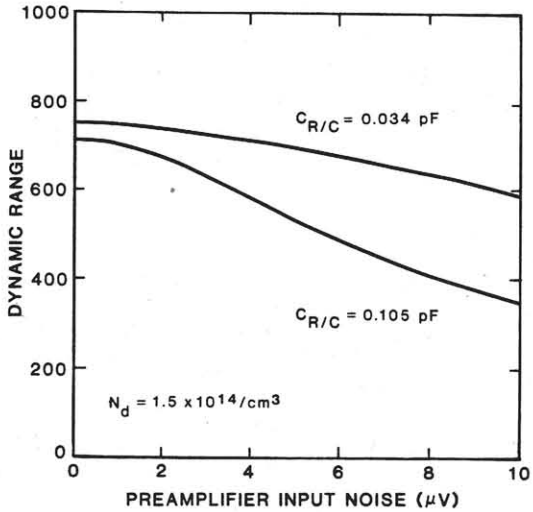

Figure 3: Plot of Output Dynamic Range vs Preamplifier Input Noise Voltage for 128 x 128 array.

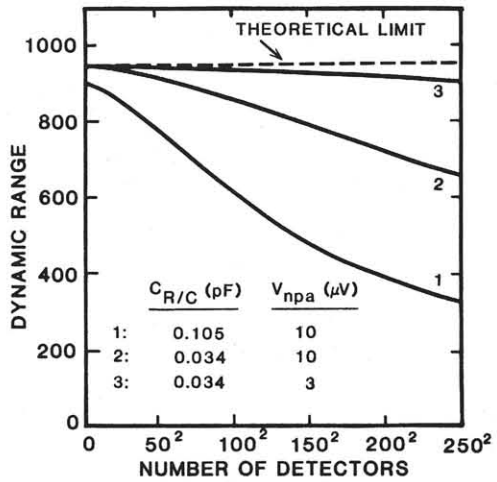

Figure 4: Output Dynamic Range vs Array Size.

Experimental evaluation of the relative improvement in performance was made by performing charge transfer experiments on 128 x 128 arrays. In these experiments, charge is integrated under a column site, and at the end of the integration time, an appropriate row is driven to deep depletion to transfer charge from the column to the row site. This charge transfer results in a change in the column voltage, which is measured. Figure 5 shows measured output signal plotted versus column–to–substrate bias voltage for CID5 and CID3. The new design, CID5, shows a much larger output signal than our older design. However, the relative magnitude of the change is larger than expected, which leads us to believe that the charge capacity in the new arrays is also significantly higher than calculated. Several design and process–related factors can contribute to the higher output signal: lower than expected row–to–column overlap capaci-

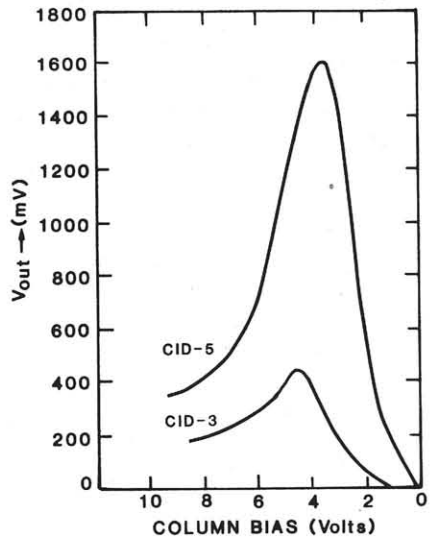

Figure 5: Measured Array Output Signal vs Column Voltage.

tance, larger active area, higher deep depletion electric field, improved gate oxide, and lower substrate donor concentration. All of these, except the reduced overlap capacitance, result in increase charge capacity. Additional studies are in progress in order to determine the relative contributions of the above factors.

Spectral response measurements were made on the new arrays as well as on the previous ones. Both types had very similar photo–response characteristics and showed the anticipated 5.5μm cut–off wavelength. Figure 6 shows a typical spectral response of a 128 x 128 CID5 array. A very flat response has been obtained in the 3 – 5μm spectral region. Note that the data are normalized to the peak value.

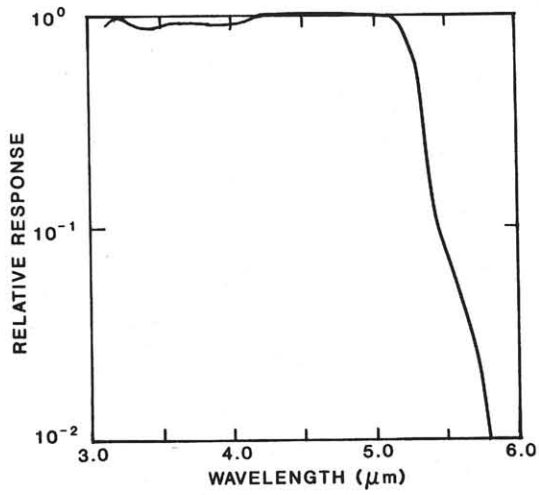

Figure 6: Measured InSb FPA Detector Photoresponse in Volts/Photon. Normalized to Peak Value.

4. STARING THERMAL IMAGERY

The 128 x 128 array has been integrated with silicon row–driver and analog readout chips on a hybrid substrate for demonstration of thermal imagery. The focal plane substrate was cooled to 77K in a dewar. Out–of–dewar electronics were the same as described previously.[3] The system was used to record thermal imagery of aircraft landing at the Los Angeles airport. Figure 7 shows photographs of some IR video imagery. Only a single frame of data is shown, with compensation provided for offsets on a pixel–by–pixel basis. However, no corrections for responsivity and gain variations have been made.

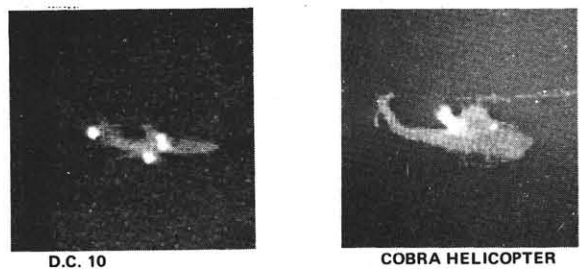

Figure 7: Images of Commercial Aircraft at Night.

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