Prototype Josephson Logic LSIs

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Suitable configurations of Josephson logic LSIs for computer applications are discussed. It is indicated that gate arrays are particularly suitable for realizing custom logic functions because of their simplified designing capability. A Josephson-threshold-logic circuit is proposed to form standard logic functions in the optimal structure. Two Josephson logic LSIs are developed: a 3K gate array and a 4x4 bit multiplier. The switching times of the OR and AND gate on the gate array were 15ps and 30ps, respectively. The critical-path delay of 210ps was attained on the multiplier.

1. Introduction

It is anticipated that Josephson devices will realize high performance beyond the ultimate capability of semiconductor devices. A number of Josephson logic LSIs have been developed [1-4]. They have achieved higher performances than any other related devices.

Computers are composed of various and many logic circuits. In order to attain high performance, highly integrated LSIs are employed in the computers. Computer logic is a combination of custom logic and standard logic. Each logic function should be realized as suitable for LSI configurations. However, because of rapid developments in the field of Josephson devices, their suitability relative to LSI configurations for computer applications has not yet been clarified. This article describes two Josephson logic LSIs which are well suited to computer logic applications: a 3K gate array and a 4x4-bit multiplier.

2. Josephson 3K gate array

The gate array is an integrated circuit in which the Josephson devices are arranged in regular order. The array is capable of realizing any kind of logic function. These functions can be modified simply by changing the wiring between the devices.

Consequently, gate arrays are convenient to realize custom logic function blocks in computers. However, the resulting logical structure is not always the optimal one.

The prototype Josephson gate array was composed focusing on high integration and easy-designing capability of logic functions. An array structure is shown in Fig.1. The array utilizing 16x34 logic cells, totaling 544 cells, is arranged on a 9x10mm chip. Each logic cell consists of four magnetically-coupled Josephson interference.

Fig.1 Structure of the gate array.
devices as OR gates and two direct-coupled Josephson devices as AND gates in the area of 240x500um². Circuit diagrams of these two devices are shown in Fig. 2. The AND gate employs a new circuit consisting of 3 Josephson junctions and 7 resistors. Because the threshold characteristics of the AND gate is nearly ideal, this circuit is effective in widening the operating margin of the LSI. The chip has 3264 gates, containing approximately 23,000 Josephson junction and 21,000 resistors. Signal pads and power pads are located around the chip. Power is supplied to each logic cell from 8 power pads through power buses. The power dissipation of the OR gate is set at 2uW, the estimated power dissipation is approximately 12mW/chip.

Prototype Josephson gate arrays were fabricated using the conventional Nb/Nb oxide/Pb-alloy Josephson junction process[5], as shown in Fig. 3. The Josephson junction size is 1.5x1.5um² and the maximum supercurrent density is 5kOAm². In order to confirm the gate array performance, the cascade chain of 154 AND gates and the cascade chain of 419 OR gates are composed on the LSI. Each cascade chain consists of multiplexers and a current detector. Utilizing the multiplexers and the current detector, the switching delay time of different stages can be measured. The switching speed measured for a 419-gate-OR-chain was 15ps/gate at a gate-bias of 96% as shown in Fig. 4. Similarly, the switching speed was 30ps/gate for a 154-AND-gate-chain.

3. 4x4-bit Josephson multiplier

The multiplier is representative of standard logic in computers. Because it is not necessary to modify this kind of logic

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Fig. 2 Circuit diagrams of OR and AND circuits.

Fig. 3 Photograph of the 3K Josephson gate array.

Fig. 4 Switching waveforms of a 419-gate-OR-chain.
function, the multiplier can be formed in the optimized LSI configuration. For this purpose, a new Josephson-Threshold-Logic circuit is employed. The concept of threshold logic is not a recent one. It has been used, for example, as the model of the neuron. The threshold-logic-circuit has plural input-signal-lines with binary signal and an output-signal-line with the binary signal, as shown in Fig. 5.

The operation of the threshold-logic-circuit is as follows. When the weighted sum of the input signal exceeds the threshold value, the output is "1". Otherwise, the output is "0". Josephson devices switch abruptly from the superconducting state to the voltage state when the input current or magnetic flux exceeds the threshold. It is not difficult to produce the weighted sum of input signals with either the current or the magnetic flux. In this sense, the threshold-logic-circuit is suited for the logic circuit by the Josephson devices.

The Josephson-threshold-logic-circuit can be realized by using the magnetically-coupled interferometer and the direct-coupled device, as shown in Fig. 6. These are a basic type and other kind of Josephson-threshold-logic-circuit can be developed by combining these basic circuits.

Utilizing these circuits, a 4x4-bit Josephson multiplier was designed focusing on high speed operation. Dual-rail configuration was adopted for this purpose. In principle, the one-bit full-adder circuit consists of 4 Josephson-threshold-gates: two carry generators and two sum generators, as shown in Fig. 7. Actually, two additional carry amplifiers were used to generate the weighted signal of the carry signal without delaying the fast carry signals, as shown in Fig. 8. The 4x4-bit Josephson multiplier shown in Fig. 9 was fabricated using the 1.5um-square Nb/Al oxide/Pb alloy Josephson junction process.

This multiplier consists of 12 adder circuits and 32 partial-product circuits. The total number of devices is 104. This number is one fourth of the number in a conventional case employing Josephson OR and AND gates. The entire multiplier is a parallelogram of 2.3mm in width and 3.1mm in height. This inclined structure was selected to decrease critical path delay. The delay
time was measured using a Josephson sampler located on the chip. The critical path which includes 11 stages of threshold gates was selected in the operation of 1111x0101 in a binary code. The critical path delay of 210ps was attained at a power dissipation of 3mW/chip, as shown in Fig.10. This operating speed is higher than that of any other multiplier circuit.

4. Conclusion

Two configurations of Josephson logic LSIs were evaluated for computer applications: the gate array LSIs and the standard logic LSIs. In conclusion, the gate array is well suited to realize custom logic functions. Standard logic LSIs should employ suitable logic circuits for each logic function to realize optimal logic structure. For this purpose, the Josephson threshold logic circuit was employed for the multiplier. The 3K gate array and the 4x4-bit multiplier were fabricated by the Nb/Pb-alloy process. Switching operations of each LSI were successfully observed. The switching times of the OR and AND gate on the gate array were 15ps and 30 ps, respectively. The critical-path-delay of 210ps was attained on the 4x4-bit multiplier. This operating speed is higher than that of any other circuit.

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References

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Fig.8 Circuit diagram of advanced one bit full-adder.

Fig.9 Photograph of the 4x4 bit multiplier.

Fig.10 Switching waveform of the multiplier.