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Heterojunction Bipolar Transistors Fabricated by Emitter and Base Self-Alignment Techniques

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AlGaAs/GaAs heterojunction bipolar transistors (HBT's) have been atracting much interest as candidates for microwave and high speed switching applications.[1-4] The high performance of ft =40GHz, fm =26GHz has already been attained.[2] A much higher performance of ft, fm > 100GHz is expected theoretically.[1]

To attain the higher performance, including a high integration, it is required to optimize the device structure as well as the heterostructure, as follows : (1) to make the size of emitter (E), Base (B) and collector (C), especially C-size to reduce B-C extrinsic capacitance (C_{BC}) ; (2) to reduce external B-resistance (R_B), and (3) to make planar HBT's for a high integration. To reduce R_B and C_{BC}, the following methods have been applied : (1) to increase the thickness of an external p^+- area by ion implatation (II) of Be^+ or Mg^+ [2,4] ; and (2) to decrease the distance between E-and B-contacts[3] ; (3) to make C-size smaller by II of O^+ [2] ; and (4) to make inverted C-up HBT's with small C-size.[4] Planar HBT's with E's of 4 μm width have been fabricated, by forming contact and connection metals by ordinary methods.[4] However, it has beenvery difficult to make planar HBT's with much smaller size, satisfying the above technical conditions at the same time.

This paper describes new, substantially planar HBT's which have very small size E's of 1μm width, connections on the same plane, and a very small distance between E-and B-contacts, and hence which make a high integration possible, and related techniques.

Fig. 1 shows a MBE-grown multi-layered structure which was used to fabricate HBT's. The newly-developed process of HBT's is shown in Fig. 2. The process is characterized by two new methods : (1) an E-self-alignment (E-SA) technique which makes it very easyto form E-contacts as described below and can be connected with II processes which need high temperature anneal, and (2) a B-self-alignment (B-SA) technique which thisE-SA technique makes possible. The fabrication is carried out, as shown in Fig. 2. First, the outside area adjacent to part in which HBT's are formed, is changed into semi-insulating (SI) area by II of O^+ or B^+, and dummy E's of SiO_2/Metal stretching from E's to the SI area are formed by dry etching (DE) of interlaid SiO_2 passivation film (Fig. 2(a)). Using the dummy E's for masks, E-mesas are formed by wet etching (WE) and small C's are formed by II of O^+ (Fig. 2(b)). In the case that n^+-cap mesas are formed, it is inevitableto make thick external p^+-B area by II of Be^+ or Mg^+, after making small C's by II of O^+ (Fig. 2(b')). E-contacts are formed by self-alignment, by coating the surface with photoresist, exposing the tops of dummy E's by DE, removing the dummy E's by WE, and evaporating E-contact metals, and subsequently C-contats are formed (Fig. 2(c)). The devices are isolated from each other by II of H^+, and SiO_2 side walls are formed by using umbrellas of E-contact metals which are formed by undercutting by WE and by DE of SiO_2 film which covers the surface (Fig. 2(d)). B-contacts are formed very close to E's by self-alignment, by evaporating B-contact metals and removing the SiO_2 side walls by WE (Fig. 2(e)). Finally, connection metals are formed as Fig. 2(f) .

In this process, B-contacts are effectively formed, because a mushroom type of SiO_2 side walls prohibit E-and C-contact metals from contacting with each other. The processes of II of O^+ and Be^+ or Mg^+ which need high temperature anneal can be easily introduced, beccause the dummy E's of SiO_2 are placed on E's at these processes. The newly developed techniques can be applied to the C-up HBT's also.

Fig. 3 shows a photograph of a fabricated planar-like HBT with E-width of 1μm, by using AuGe/Ni/Ti/Au for E-and C-contacts. AuZu/Au for B-contacts, H^+ for devices isolation from

each other, and O^+ for making adjacent SI area. Fig. 4 shows a DC property of this device. Planar-like HBT's which operate in the region of > 40GHz are expected.

References :

1) H. Kroemer, Proc. IEEE 70, 13(1982).
2) P.M. Asbeck etal., IEEE, EDL-5, 310(1984).
3) K. Nagata etal., Annual Abst. of IECE of Japan 10, 2-370(1985).
4) K. Tsuda etal., ED 84, 67(1984).

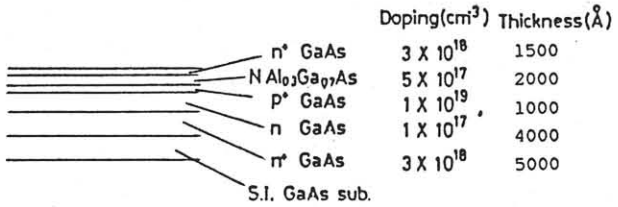

Fig. 2. MBE-grown multi-layered structure used for HBT's.

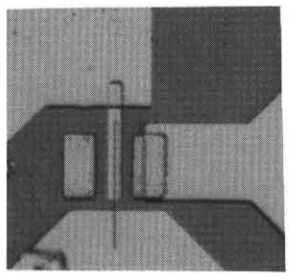

Fig. 3

A photograph of a planar HBT with emitter width of lum.

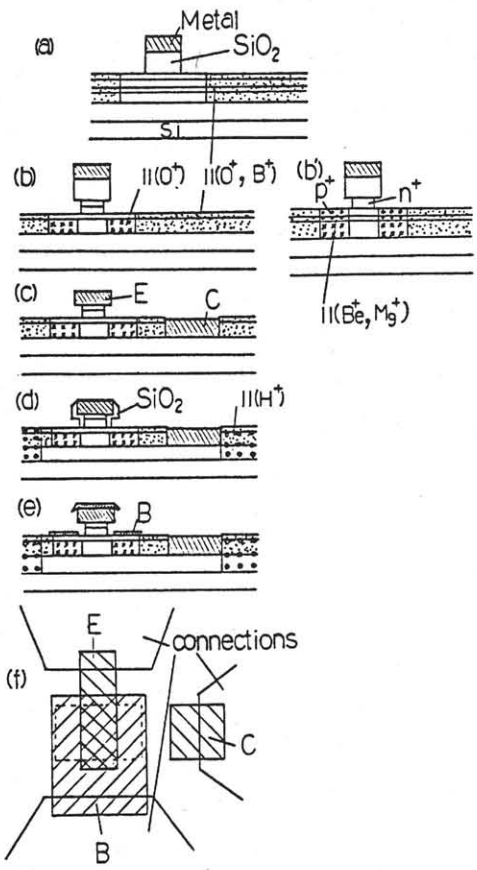

Fig. 1

Fabrication process of planar HBT's by emitter and base selfalignment techniques.

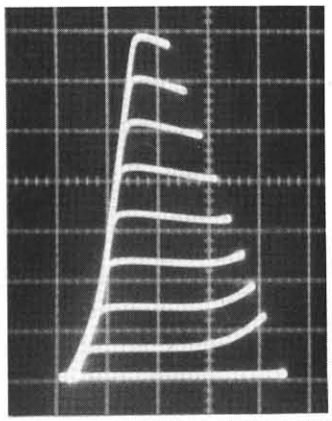

Fig. 4 (V:1mA, H:2V, S:200μA)

A DC property of a planar HBT with emitter width of lum.