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Nanometer-Scale Silicon MOSFETs

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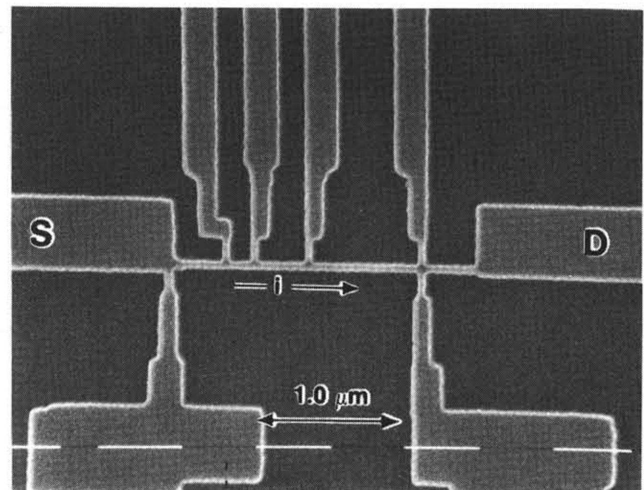
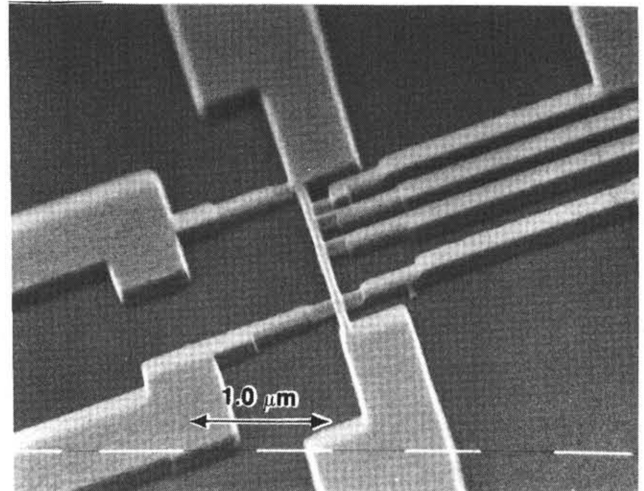
Using a combination of new microfabrication techniques together with conventional processing, we have made silicon MOSFETs with channels only a few tens of nanometers wide. Since they are clean, well characterized, and have a variable electron density controlled by the gate, these devices are excellent for studying electron transport in small structures. These small transistors have been used to study one-dimensional conduction and a variety of new quantum transport and single electron effects.

Recent advances in high resolution fabrication have made possible silicon MOSFETs with critical dimensions as small as several tens of nanometers [1,2,3]. These devices have been used as nanolaboratories for the study of electron conduction in one-dimensional structures where quantum transport and single electron effects are important. Understanding the conduction processes in these nanostructures is important for defining the fundamental limitations of existing devices and, perhaps, for providing clues to fruitful directions in the search for new devices.

A silicon MOS inversion layer is a two-dimensional electron gas that can easily be formed into complex shapes by simply patterning the gate electrode. The transistors used in our electron transport experiments are n-channel polysilicon gate devices with refractory metal contacts made using optical lithography for all but the final gate pattering. This high resolution step is done with electron beam lithography and plasma etching, leading to final linewidths as small as 20 nm. The gate geometry of these devices generally



1a)



1b)

Figure 1 Top and side view of 40 nanometer wide silicon MOSFET.

comprises long, narrow sections with probes along the edge for monitoring local potentials.

An example of such a device is shown in Fig. 1. The upper micrograph is a top view of the gate of a completed device. The current flows from the source on the left to the drain on the right through the narrow (40 nm) channel segment. The lower micrograph is shows a perspective view of the same device. The metal layer, patterned using electron beam lithography, acts as a mask for reactive ion etching of the underlying polysilicon gate, the gate oxide, and the silicon substrate. By forming a pedestal in the substrate, the electron gas can accurately confined to a region directly under the gate electrode.

At room temperature, even these small devices behave like conventional MOSFETs, but at low temperatures, a variety of novel effects become important. The region between two probes in Fig. 1 is only about 10–10cm², an area small enough that it should contain only a few tens or hundreds of conduction electrons and, also, only tens or hundreds of oxide interface traps. For these reasons, discrete conductance effects should be easy to observe.

Figure 2 shows the conductance of such a channel as a function of time. The characteristics are dominated by a random switching of the conductance between two well defined states. These states correspond to a single electron being captured by a single oxide interface state between the center two probes in the region labeled "B" in the figure. Note that the effect of the change in scattering for electrons in the channel caused by this single event is easily measured and also that it is delocalized enough that it can be observed between voltage probes several tenths of microns away from the trapping site (regions "A" and "C" in the figure).

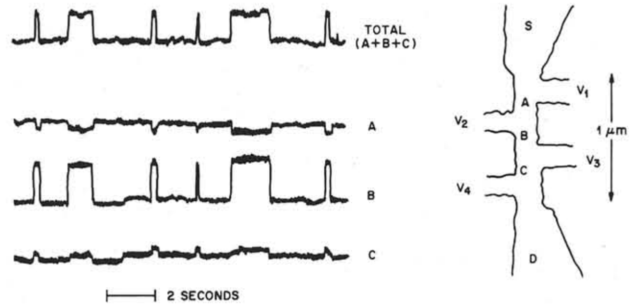


Figure 2 Conductance switching in MOSFET channel due to filling of a single interface trap.

The nonlocal nature of the scattering events shown in Fig. 2 is related to the more general phenomena of universal conductance fluctuations for which these MOSFETs are almost ideal test structures. Classically, electron conduction is determined by the number and strength of scattering sites. In a system with a small number of scatterers and an electron coherence length approaching the sample size, interference effects associated with the electron scattering events become important. This interference will give the sample a distinctive conductance "fingerprint" that will vary between nominally identically samples or in a single sample when the position of the scatterers is changed or a magnetic field is applied. Recent theory has predicted that the magnitude of the conductance fluctuations scales as the ratio of the sample size to the inelastic scattering length [4]. When these lengths are comparable, the fluctuations will be of order e^2/h.

Measurements on these small MOSFETs have been made over a wide range of sample sizes and inelastic scattering lengths [5]. The magnitude of the conductance fluctuations as a function of magnetic field (δg) has been compared with theory using only the inelastic scattering length and sample size as parameters. Figure 3 shows the excellent agreement between the measured and predicted fluctuation magnitude over three decades in conductance.

Combining high resolution patterning techniques with variable electron density controlled by a gate has made Si MOSFETs a powerful tool for studying quantum transport effects. Extending this technology to other material systems, like GaAs, should further expand our knowledge of electron transport in small systems.

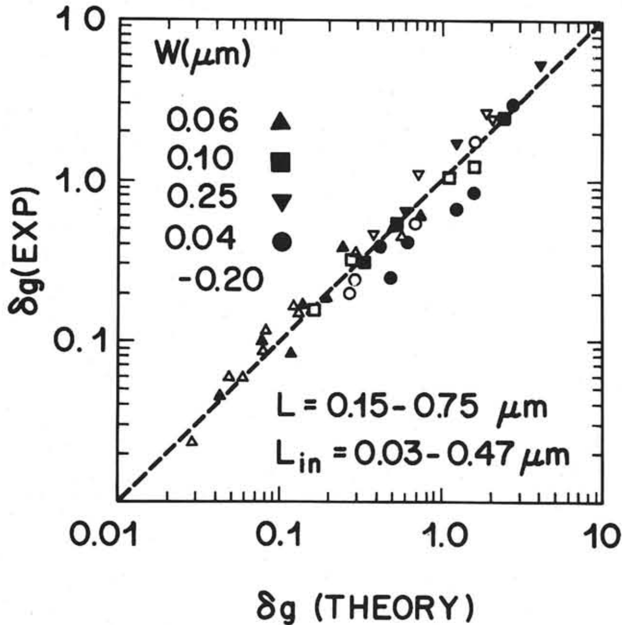


Figure 3 Magnitude of magnetoconductance fluctuations in small silicon MOSFET.

References

[1] R.E. Howard, L.D. Jackel, P.M. Mankiewich, and W.J. Skocpol Science, **231**, 346-349, (1986).

[2] P.M. Mankiewich, R.E. Howard, L.D. Jackel, W.J. Skocpol, D.M. Tennant, J. Vac. Sci. and Technol., **B4**, 380-382, (1986).

[3] R.E. Howard, W.J. Skocpol, L.D. Jackel, P.M. Mankiewich, L.A. Fetter, D.M. Tennant, and R.W. Epworth, IEEE Trans. Elect. Devices, **ED-23**, 1669, (1985). P.A. Lee and A.D. Stone, Phys. Rev. Lett. **54**, 2692, (1985).

[4] W.J. Skocpol, P.M. Mankiewich, R.E. Howard, L.D. Jackel, D.M. Tennant, Phys. Rev. Lett., **56**, 2865-2868, (1986).