Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 5-9

Invited

BiCMOS Process and Device Technology for High Speed VLSIs

Takahide Ikeda

Device Development Center, Hitachi Ltd.

2326, Imai-cho, Oume-shi, Tokyo, 198, Japan

Hi-BiCMOS(high-performance bipolar CMOS) process and device technology is reviewed. High speed bipolar transistors can be fabricated on the same chip with standard CMOS with minimum additional process steps. 1.3μm technology has been applied to develop SRAMs, gate arrays and a DRAM test chip. They exhibited speed about twice as fast as CMOS. Future of BiCMOS technology is also discussed.

1. Introduction

Recently, CMOS has become the main technology for high packing density VLSI due to its inherent low power characteristics. Higher packing density will be possible once improvements have been made in fine pattern lithography. However, CMOS circuit delay is limited by the poor driving capability of MOSFETs compared with bipolar transistors. Progressive increase in speed will level off because of the various limitations on the scaled down MOSFETs, such as saturation velocity of carriers, hot carrier problem, parasitic resistance, etc.

In the field of ultra-high speed LSI, bipolar technology is still essential due to the advantage of high current driving capability and good threshold control. However, integration density is limited by power dissipation and the yield problem. ECL gates consume about one order of magnitude more power than CMOS gates.

BiCMOS technology has great potential to fill the gap between CMOS and bipolar technology. It can produce VLSI which possesses high speed characteristics of bipolar LSI and the low power, high packing density characteristics of CMOS VLSI.

Two technologies have been essential to the development of BiCMOS VLSI. One is the circuit technology to combine bipolar transistors effectively with CMOS circuits. The other is the process and device technology necessary to fabricate high performance bipolar transistors on the same chip as the CMOS.

One of the basic circuits of BiCMOS is the combination gate shown in Fig. 1 (1, 2). Its power dissipation is as low as CMOS gates because there is no stand by power. The driving capability is about 5 times greater than CMOS as shown in Fig. 2.

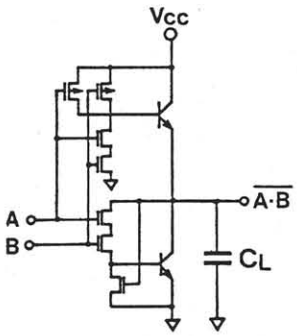
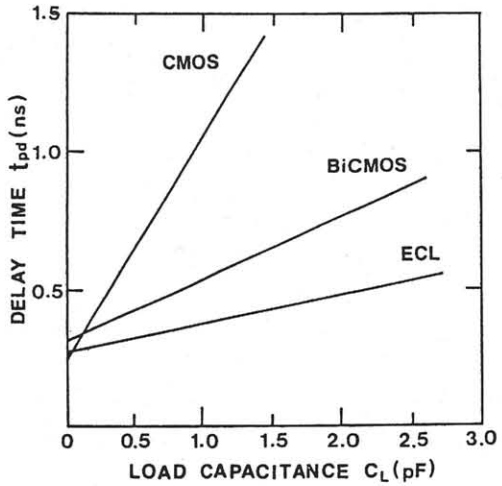


Fig. 1 2-Input NAND BiCMOS gate



2NAND, 1.3μm Technology

Fig. 2 Comparison of gate delay vs C_l

An optimized device structure has been developed which incorporates buried twin wells and the emitter fabricated by CMOS process (3). The above circuit and process technologies are called Hi-BiCMOS(high-performance BiCMOS) technology and were applied successfully to high speed static RAMs (4-7) and gate arrays (1, 8). A test chip of 1Mbit BiCMOS DRAM (9) and elementary chips for BiCMOS microprocessors (10, 12) have also been demonstrated. These VLSIs are twice as fast as CMOS VLSIs fabricated with the same lithography.

In this paper, Hi-BiCMOS process and device technology and some applications are described. Future trends of BiCMOS devices are also discussed.

2. Process and Device

BiCMOS processes and devices must satisfy the following of performance and cost requirements.

(1) small size bipolar transistor with high cut off frequency f_T.
(2) minimum additional process steps.
(3) fully compatible process with standard CMOS.

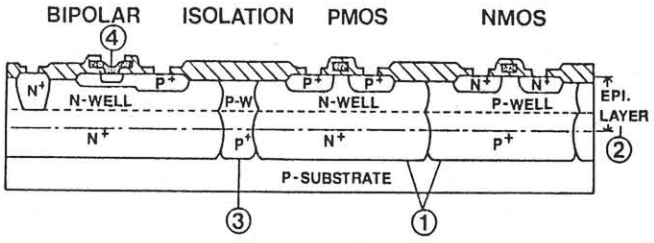
To meet these requirements, the Hi-BiCMOS device structure shown in Fig. 3 has been developed. Fig. 4 shows the process sequence designed on the base of double poly-silicon CMOS process for SRAM. To obtain high f_T at high current density, thin epitaxial layer substrate with buried layers is essential.

One prominent feature of the structure is the N^+/P^+ buried twin well combined with the surface twin well. By controlling the well profile, MOSFETs can be fabricated in the epitaxial layer thin enough without degrading device characteristics, as shown in Fig. 5. Narrow isolation between bipolar transistors is achieved by the LOCOS and the P^+ buried layer.

High f_T bipolar transistor emitter can be fabricated using the basic CMOS process. The poly-silicon emitter structure shown in Fig. 2 is made using a second poly-silicon layer in the CMOS process without additional process steps.

In BiCMOS DRAM, emitter is formed by the N^+ layer of the NMOS source and drain in terms of process compatibility. An f_T of 5.2GHz is obtained from the optimized layout and impurity profile (12).

Additional process steps for bipolar in Fig. 4 are N^+/P^+ buried layer fabrication, epitaxial growth, collector and base ion implantation. The number of steps is increased by less than 30%.



① N^+/P^+Buried Twin Well
② Thin Epitaxial Layer (N^-, 1-1.5μm)
③ LOCOS + P^+Buried Layer Isolation
④ Poly-Si Emitter of 1μm Width

Fig. 3 1.3μm Hi-BiCMOS device structure

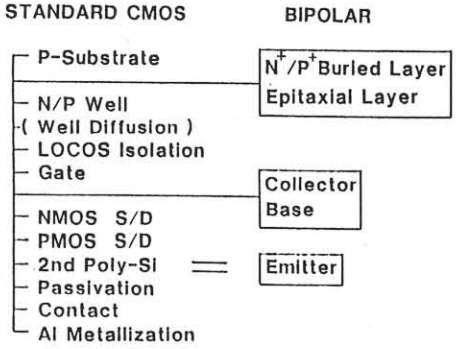
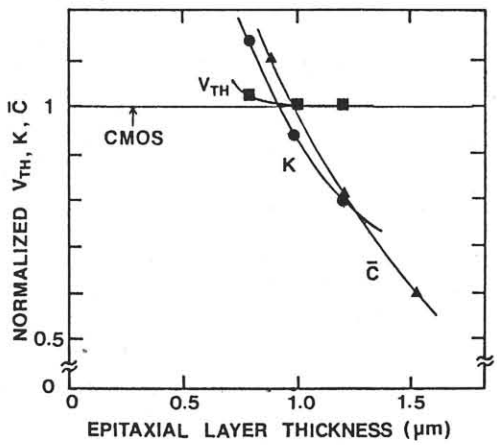


Fig. 4 Process sequence



V_{TH}: Threshold Voltage, K: Body Effect Constant
$\bar{C}$: Average Junction Capacitance (0 - 5V)

Fig. 5 NMOS characteristics vs epitaxial layer thickness

The buried layer of Hi-BiCMOS devices also has two advantages over conventional CMOS. One is the improvement of latch up immunity due to low well resistance. The well triggering current is one order of magnitude larger than that of N-well CMOS.

The other is the improvement of soft error immunity. Fig. 6 shows the soft error rate for the bit line mode obtained from the 1Mbit Hi-BiCMOS DRAM test chip. It is less than one twentieth of the CMOS DRAM chip (12).

Major characteristicses of 1.3μm Hi-BiCMOS device are summarized in Table 1.

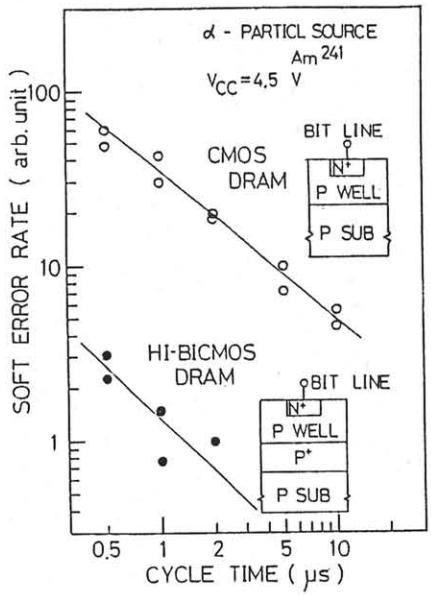


Fig. 6 Bit line mode soft error rate of Hi-BiCMOS DRAM

Table 1 Device characteristics of 1.3μm Hi-BiCMOS

Device		Characteristics	Value	Unit
Bipolar	Emitter= 1x2 μm²	h_{FE}	100	—
		BV_{CEO}	8	V
		BV_{CBO}	17	V
		R_{CS}	180	
		f_T	6	GHz
		C_{EB}	11	fF
		C_{CB}	15	fF
		C_{CS}	135	fF
NMOS	W/L= 15/1.2 μm/μm	V_{TH}	0.55	V
		BV_{DS}	10	V
		βomax	80	μS/V
PMOS		V_{TH}	−0.55	V
		BV_{DS}	20	V
		βomax	27	μS/V

3. Application to VLSI

High speed memory is one of the most promising applications of this technology. As a typical example, configration of Hi-BiCMOS 64Kbit ECL RAM is shown in Fig. 7. An NMOS memory cell with a high resistor is adopted due to its low power dissipation and small cell size. The BiCMOS decoder and driver, bipolar sense amplifier and ECL I/O buffer are used to attain high speed access time.

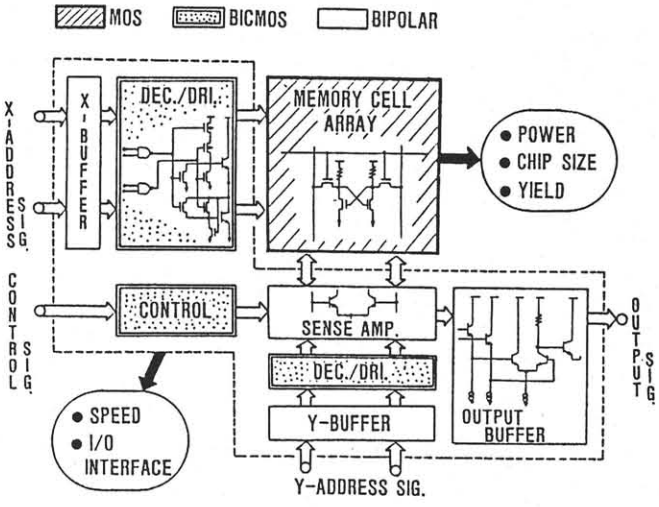


Fig. 7 Configuration of Hi-BiCMOS ECL RAM

A Typical access time of 7ns is obtained by 1.3μm technology. The access time is comparable to bipolar ECL RAM, its chip size is 1/2 and power dissipation is 1/2-1/3.

As for the TTL interface, a 256Kbit SRAM exhibited 15ns typical access time with comparable chip size and power dissipation to the CMOS.

In the 1Mbit Hi-BiCMOS DRAM test chip, a typical access time of 35ns is also half of CMOS DRAM.

Fig. 8 shows the trend of BiCMOS SRAM. It has acquired a new market in the high speed version of CMOS SRAM and high density version of ECL RAM.

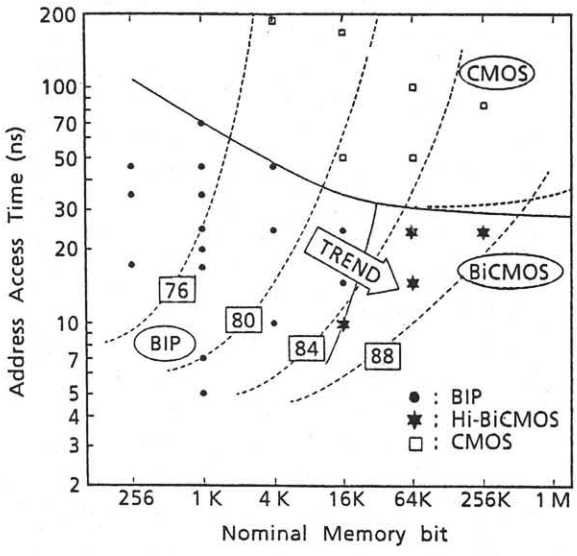


Fig. 8 Trend of Hi-BiCMOS SRAM

As an application to logic VLSIs, a sub-nanosecond gate array with a 7Kgate and 4.6Kbit RAM has been developed. Gate delay is 0.45ns at 0.6pF and power dissipation is 0.23mW at 10MHz. The gate delay is one half of the CMOS gate array and is twice that of the ECL gate array.

High speed microprocessor is another promising application. As key components of the processor, macrocell test chips such as ALU, ROM, 64bit multiplier, etc. have been demonstrated (10, 11). A machine cycle of 25 ns is expected using 1.3μm technology.

Process technology for logic VLSI is the same as that of SRAM except for the process steps of memory cell fabrication.

4. Future of BiCMOS

Improvement of the delay time of the basic gate due to the scale down is expected. Table 2 is the approximate expression of tpd with the load capacitance C_L and key device parameters (13). BiCMOS gates have the advantage that tpd depends on the square root of C_L. In BiCMOS gates, intrinsic cut off frequency f_{Ti} as well as gm of MOSFET are the key parameters.

Fig. 9 shows key parameter trends. Drain current of MOSFET is almost constant when both gate length and width are scaled down. f_{Ti} has the potential to be improved by shallower junctions as are already used in high speed bipolar technology.

Fig. 10 shows trend of the basic gate delay time and the access time of 64Kbit ECL RAM. The lower curve of the delay time corresponds to the scale down of compaction shrink and upper curve to that of constant chip size. When packing density increases due to the scale down of the device and chip size is constant, C_L is not reduced by a scale factor. The superiority of BiCMOS gate in that case is remarkable.

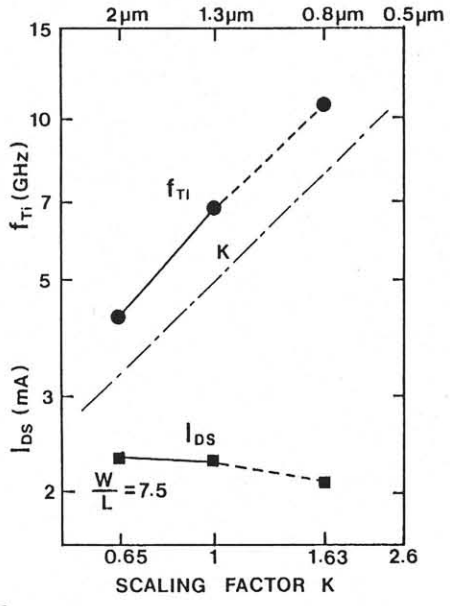
The access time of 64Kbit ECL RAM is also improved approximately by scale factor K as shown in Fig. 10.

At 0.5μm, if the supply voltage drops to 3.3V, the trend in Fig. 10 will shift both in CMOS and BiCMOS. To maintain the trend it will be necessary to optimize circuit configurations as well as device structure which are suitable for low supply voltage.

For still higher speed in future BiCMOS VLSI, higher f_T and smaller size bipolar transistors are required. High speed bipolar technologies such as self-alignment and deep isolation will be required to be merged with CMOS technology within reasonable additional process steps.

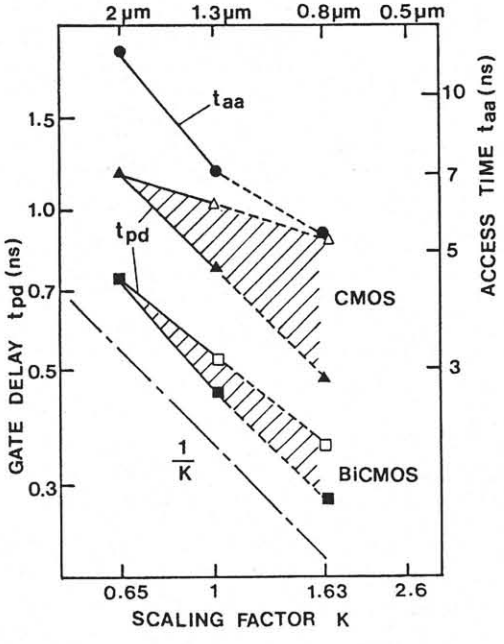
Table 2 tpd of CMOS and BiCMOS
gm = Ids/Vcc

CMOS	$\frac{C_L}{2g_m}$
BiCMOS	$\frac{C_L}{\sqrt{2\pi f_{Ti} g_m}}$



f_{TI} : Intrinsic Cut Off Frequency of Bipolar
I_{DS} : Drain Current of NMOS ($V_G = V_D = 5V$)

Fig. 9 Trend of f_{Ti} and drain current of NMOS



taa : Access time of 64Kbit ECL RAM
tpd : Gate delay of CMOS and BiCMOS 2-NAND, same gate area

Fig. 10 Trend of access time and gate delay

Finally Fig. 11 shows the trend of process complexity with the year when products first come into the marketplace. The weight of the additional processes will become relatively small because CMOS requires more complex processes to fabricate finer patterns and to improve reliability. The difference will become very small if CMOS adopts epitaxial substrates.

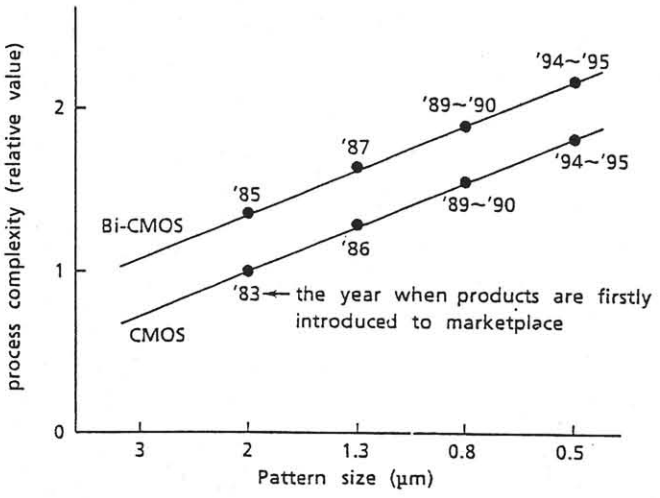


Fig. 11 Process complexity vs pattern size

5. Conclusions

Hi-BiCMOS process and device technology which can fabricate high performance bipolar transistor on the same chip with the standard CMOS has been developed. Hi-BiCMOS VLSIs such as SRAMs, DRAM, gate array, etc. have been developed using this technology. This technology can produce VLSIs that are about twice as fast as CMOS, and VLSIs having higher packing density than bipolar LSIs with comparable speed and low power characteristics.

Due to trends in device performance, higher f_T and smaller size bipolar transistors are required. In the future, leading-edge technology of bipolar and CMOS will be merged for high speed applications, and much wide applications will unfold.

6. Acknowledgements

The author would like to thank Drs. M. Kubo, M. Yoshimura, I. Masuda, K. Miyata, K. Itoh H. Higuchi, T. Nitta, K. Ogiue for their encouragement and helpful discussions of this study.

7. References

(1) Y. Nishio, et al. ; Proc. of ICCD pp428-433 (1984)
(2) S. C. Lee, et al. ; Dig. of Tech. Papers of VLSI Symposium pp46-47 (1984)
(3) T. Ikeda, et al. ; Dig. of Tech. Papers of IEDM pp408-411 (1986)
(4) K. Ogiue, et al. ; Proc. of ICCD pp17 (1985)
(5) K. Ogiue, et al. ; Dig. of Tech. Papers of ISSCC pp212-213 (1986)
(6) S. Miyaoka, et al. ; Dig. of Tech. Papers of ISSCC pp132-133 (1987)
(7) M. Odaka, et al. ; Dig. of Tech. Papers of ECS pp403 (1987)
(8) Y. Nishio, et al. ; Proc. of CICC pp203-204 (1987)
(9) R. Hori et al. ; Dig. of Tech. Papers of ISSCC pp280-281 (1987)
(10) T. Hotta, et al. ; Dig. of Tech. Papers of ISSCC pp190-191 (1986)
(11) T. Hotta, et al. ; Proc. of CICC pp253-256 (1987)
(12) Y. Kobayashi, et al. ; Dg. of Tech. Papers of IEDM pp802-804 (1986)
(13) H. Higuchi, et al. ; Dig. of Tech. Papers of IEDM pp694-697 (1984)