Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 11-14

SCC (Surrounded Capacitor Cell) Structure for DRAM

G. Fuse, K. Tateiwa, S. Odanaka, T. Yamada, I. Nakao, H. Shimoda,
O. Shippou, M. Fukumoto, J. Yasui, Y. Naito, and T. Ohzone
Matsushita Elec. Ind. Co. Ltd. Semiconductor Research Center.
3-15 Yagumo-nakamachi, Moriguchi, Osaka, Japan

SCC structure , which is used fully tilt angle implantation into vertical sidewall, has been developed.

Large capacitance can be realized at small cell size, because of surrounded capacitor around cell and Hi-capacitance structure. A storage cell capacitance of about 100 fF is obtained with 2.2×4.6 μm^2 area and minimum size of 0.8 μm. The separation between cells can be done by simple boron implantation at the bottom of trenches.

Introduction

Trench capacitor cell is one of key technologies for high density DRAMs.[1] Cell size can further be shrunk if trenches are used as capacitors as well as isolations[2-5]. The area of one cell with switching transistor, capacitor and separation must be down to about 4 μm^2 ,to put 16 Mbit DRAM in 300 mil package. Moreover it is necessary to obtain large capacitance.

Cell structure and process steps.

Figure 1(a) and (b) show the structure of the SCC. All of sidewall n^+ regions surrounding the unit cell are used for storage node. In the cross sectional view, mark ① is the As^+ implanted connection region between source and storage node. Mark ② is the p^+ separation region between drain and storage node. Mark ③ is As^+ implanted storage node. Mark ④ is Hi-C p^+ region. Mark ⑤ is the p^+ region for cell isolation. Implantations except ⑤ are performed using the combination of tilt angle implantation and intermittent wafer rotation by 90° in order to dope uniformly sidewalls of all directions.

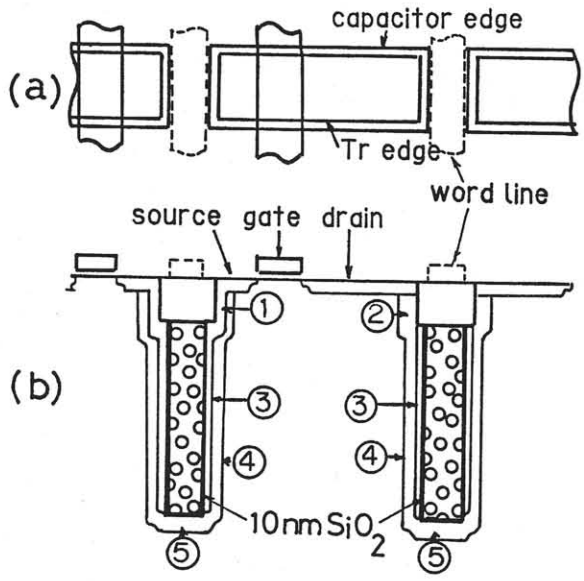

Fig.1 The structure of the SCC.

In major process steps, tilt angle implantations[6] are fully utilized to realize the SCC for precise impurity profile control (Fig. 2).

(a) First of all, shallow trenches of 0.8 μm depth are formed. At this step, As^+ implantation (Fig. 1①) and B^+ implantation

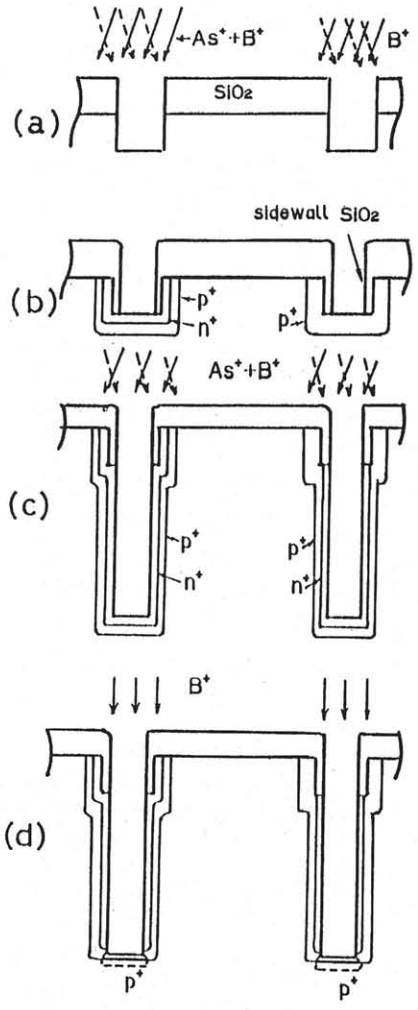

Fig.2 Process steps.

(Fig. 1②) are selectively performed. B^+ implantation is not only necessary for channel stopper, but also for suppressing n-channel MOS narrow width effect.

(b) Sidewall SiO_2 films of 150 nm thickness are formed.

(c) Silicon trenches are etched to a depth of 3.3 μm. To form Hi-C structure , the sidewall electrode is formed by double implantation of As^+ and B^+.

(d) For isolation between cells, additional etching to a depth of 0.2 μm and B^+ implantation are performed at the bottom of the trench.

After cell oxide of 10 nm are formed, polysilicon is buried into trenches as a cell plate. At the upper part of trenches, SiO_2 are buried.

Impurity profile (SIMS & simulation)

Measured impurity profiles of the Hi-C structure implanted at tilt angle of 82° are compared with simulation results (Fig. 3). The comparison has disclosed that effective dose decreased by 25 % for As^+ and 40 % for B^+ atoms, respectively, because of incident ion reflections.

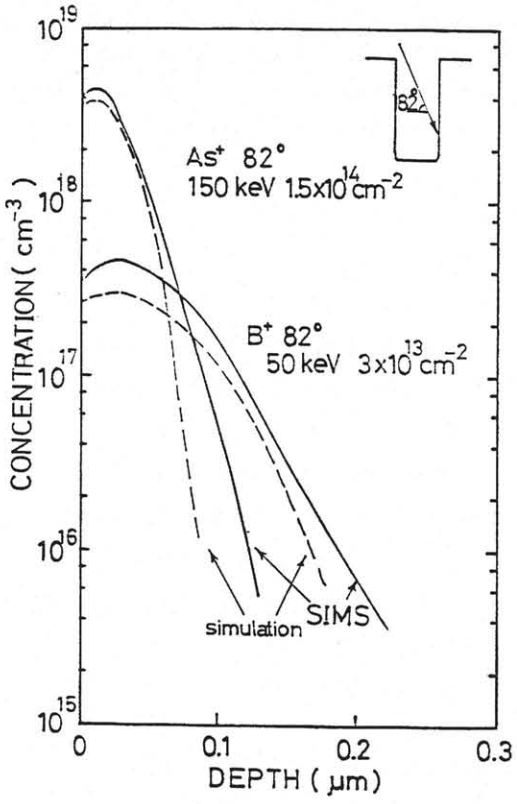

Fig.3 Impurity profiles of the Hi-C structure.

SEM observation of doping region.

Doping region at the sidewalls of trenches were observed by SEM using enhanced etching of n^+ doped regions.

Figure 4 shows the cross sectional SEM micrograph of completed memory cells. The memory cell structure shown in Fig. 1(b) was successfully fabricated.

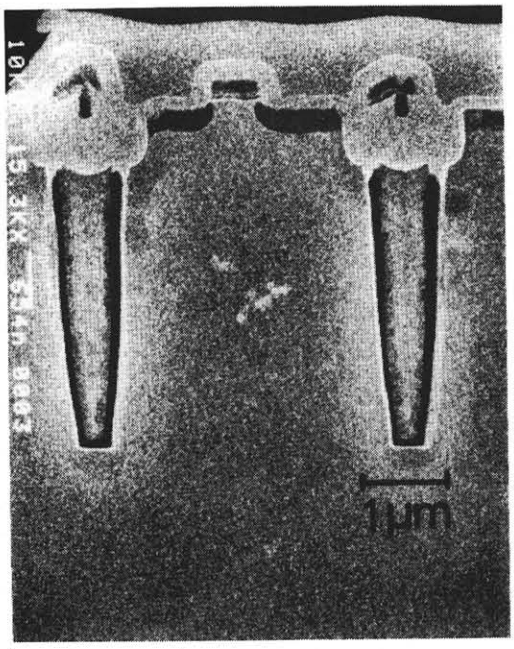

Fig.4 Cross sectional view of completed memory cell.

Electrical characteristics

The trench depth is 4.3 μm, capacitor dielectric SiO_2 thickness is 10 nm, and trench width is 0.8 μm. Cells with total peripheral length of 250 μm were fabricated for the capacitance measurements. Fig. 5 shows a characteristics of cell capacitance, which is normalized to the oxide capacitance in an accumulation mode. Storage node voltage is varied from 0V to 3V. The supply voltage V_{cc} is 3V, and the plate voltage is $1/2V_{cc}$ =1.5V, while the substrate voltage is 0V. The capacitance increase in Hi-C structure is very large at storage node voltage of 0V, but small at 3V. Total storage capacitance is the sum of C_{OX} and $C_{j(Hi-C)}$. The average capacitance is 12.3 fF / μm at 0V and 6.7 fF / μm at 3V.

Leakage current between cells is measured as a function of the cell plate voltage (Fig. 6). Additional etching of the trench bottom by 0.2 μm reduces the leakage current significantly. Threshold voltage of the parasitic MOSFET at the bottom of the cell plate remained unchanged in the separation width of 0.7-1.2 μm.

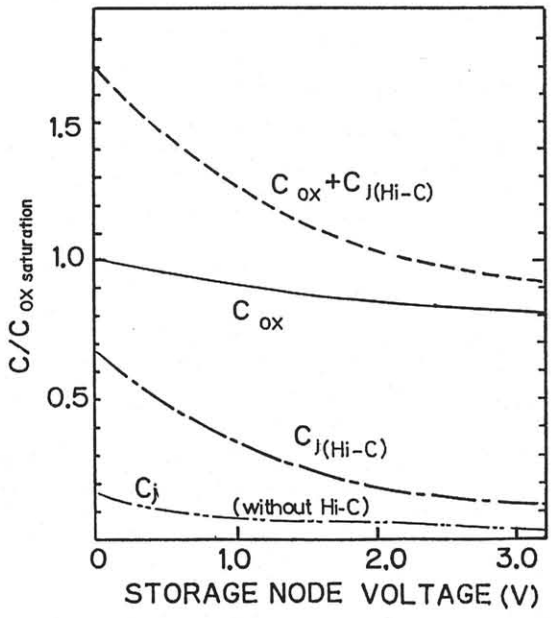

Fig.5 Characteristics of the cell capacitance. $V_{sub}=0V$ and $V_{plate}=1.5V$ C_{ox} is the capacitance between the cell plate and the storage node. $C_{j(Hi-C)}$ and C_j are the capacitances with and without Hi-C p-n junction, respectively.

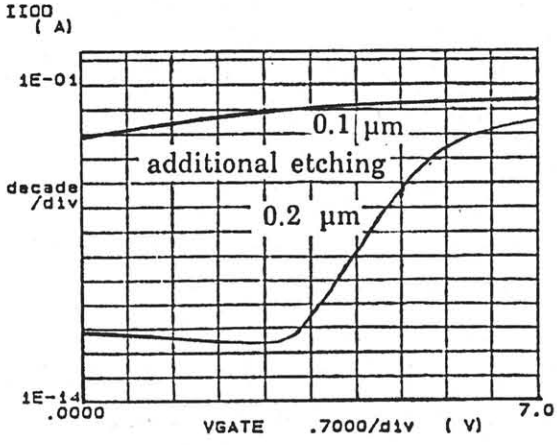

Fig.6 Leakage current between cells as a function of the cell plate voltage. (500 μm length and 0.8μm width)

The electrical characteristics of write and read modes, are shown in Fig. 7(a) for the test devices shown in (b).

A typical $\overline{RAS}$ access time of 70 nsec has been achieved in 4 Mbit DRAM.

Two dimensional potential simulation of the cell with 0.5 μm minimum feature size shows that the storage node can be separated electrically from the bit line node in the SCC by an appropriate doping (Fig. 8). 16Mbit DRAM with trenches of 0.5 μm width and 4 μm depth can be realized by 7° tilt angle sidewall implantation, while conserving cell capacitance of about 50 fF.

Conclusion

The memory cell structure of SCC was proposed for Mbit DRAMs. Experimental 4Mbit DRAM with 2.2×4.6 μm^2 cell area and minimum size of 0.8 μm was successfully fabricated. A storage cell capacitance of about 100 fF is obtained. The SCC cell can be applied to 16Mbit DRAMs if only the minimum feature size is scaled down to 0.5 μm.

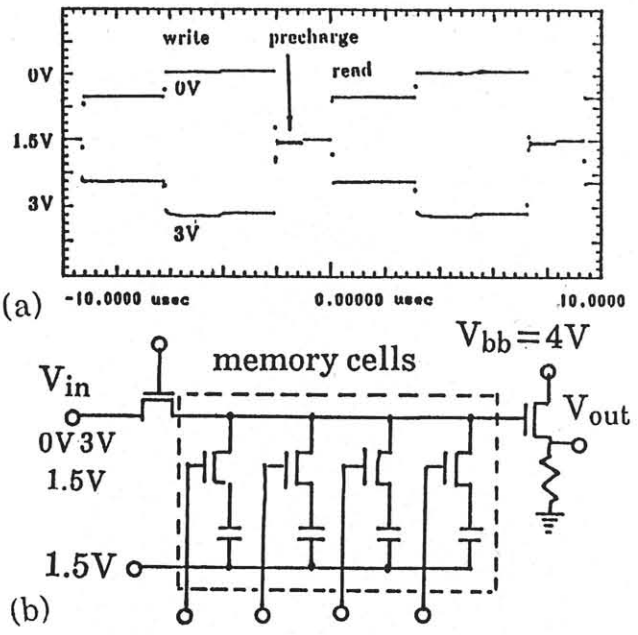

Fig. 7(a) The electrical characteristics of write and read mode.
(b) The test devices.

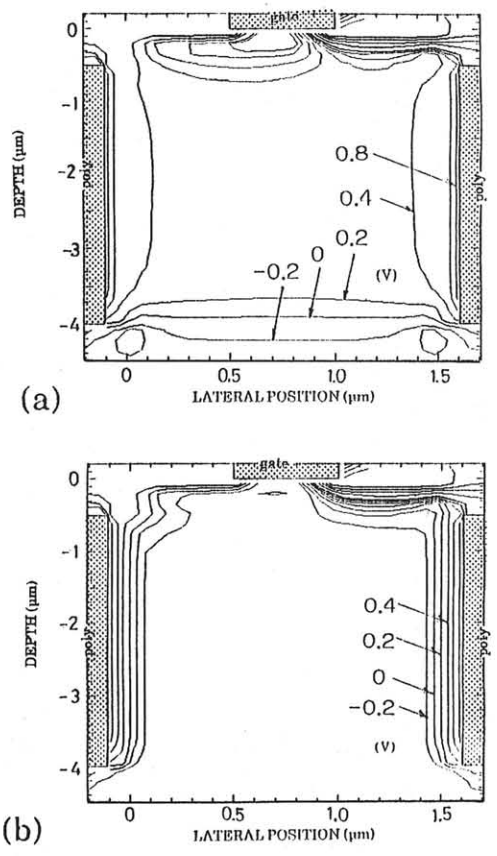

Fig.8 Potential distribusions of the SCC with 0.5μm minimum feature size(a) without Hi-C structure and (b) with Hi-C structure.

References

1)H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe, and S. Asai, IEDM Tech Digest (1982) 806.

2) K. Nakamura, M. Yanagisawa, Y. Nio, K. Okamura, and M. Kikuchi, ibid, (1984) 236.

3) S. Nakajima, K. Miura, K, Minegishi, and T. Morie, ibid, (1984) 240.

4) M. Wada K. Hieda, and S. Watanabe, ibid, (1984) 244.

5) K. Tsukamoto M. Nagatomo, Y. Okumura, T. Ogawa, Y. Matsuda, S. Osaki, and T. Matsukawa, Extended Abstracts of the 18th Conf. on Solid State Devices and Materials, (1986) 295.

6) G. Fuse, H. Umimoto, S. Odanaka, M. Wakabayashi, M. Fukumoto, and T. Ohzone, J. Electrochem.Soc.,Vol.133,No.5, (1986) 996.